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G43T-DM1

Rev: A00
Support EuP Lot 6

The EAGLELAKE module Specification :

- 1. MEMORY : 2 channel/4 DIMM DDR3 socket
- 2. SLOT : 1 PCI-E by 16 / 2 PCI-E by 1 /1 PCI
- 3. With 10 port Usb 2.0 & 4 port S-ATA 2
- 4. LAN : Relteak 10/100/1000M LAN
- 5. AUDIO : REALTEK ALC888S Audio Codec
- 6. I/O : Super I/O ITE 8755
- 7. VIDEO : VGA & HDMI

McCreary(Corporate) ,vPro
Eaglelake Q: Corporate Integrated Graphics

Boulder Creek(consumer) ,VIIV
* Eaglelake G: Consumer Integrated Graphics
Eaglelake P: Consumer Discrete Graphics

PCB	Total Thickness	Core Prepreg
BearLake	62 mil	50 mil
* EagleLake	59 mil	47 mil

[illegible][illegible]

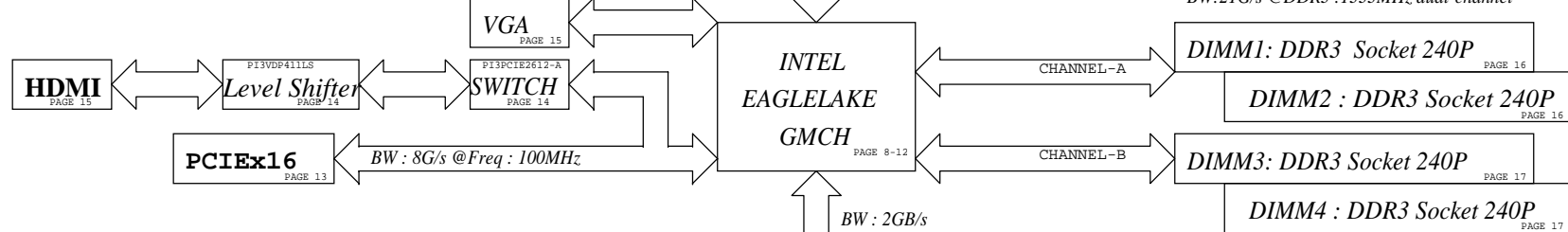
DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	A/B/C/D	PEQ1	GNT1

**INTEL
LGA 775 pin**
Intel P4 Processor Core 2 Duo
& Core 2 Quad & Dual Core
PAGE 4-6

FSB : 800MHz & Freq : 200MHz
FSB : 1066MHz & Freq : 266MHz
FSB : 1333MHz & Freq : 333MHz

BW : 10GB/s

DDR3 : 800/1066/1333MHz
BW:10.6G/s @DDR3 :1333MHz single-channel
BW:21G/s @DDR3 :1333MHz dual-channel



BW : 480MB/s @ Freq : 48MHz

PS. USBLAN is RJ45+2 port USB conn
PS. USB1394 is 1394+2 port USB conn

USBLAN
2 ports
R-USB
2 ports
USB1
2 ports
USB2
2 ports
USB3
2 ports

USB V2.0
PAGE 24

**INTEL
ICH9/10**
PAGE 19-22

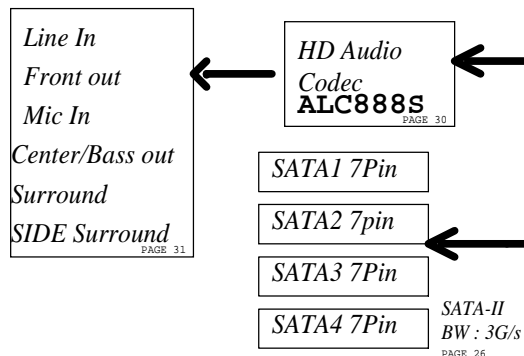
BW : 500MB/s @ Freq : 100MHz

PCIE X 1
PAGE 26
PCIE X 1
PAGE 26

**Relteak Lan
8111DL
(Giga PHY)**
PAGE 28

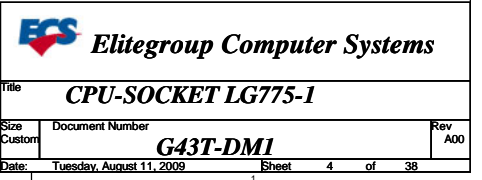
**USBLAN
RJ45**
PAGE 28

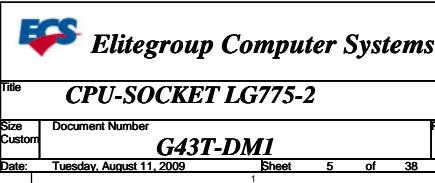
PCI Slot 120pin @ AD17
PAGE 27



PCB : 244 x 244 x 1.5 mm ; 4 layers

System Block Diagram		
Title	Document Number	
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CPU1E



VCCORE

VCCORE



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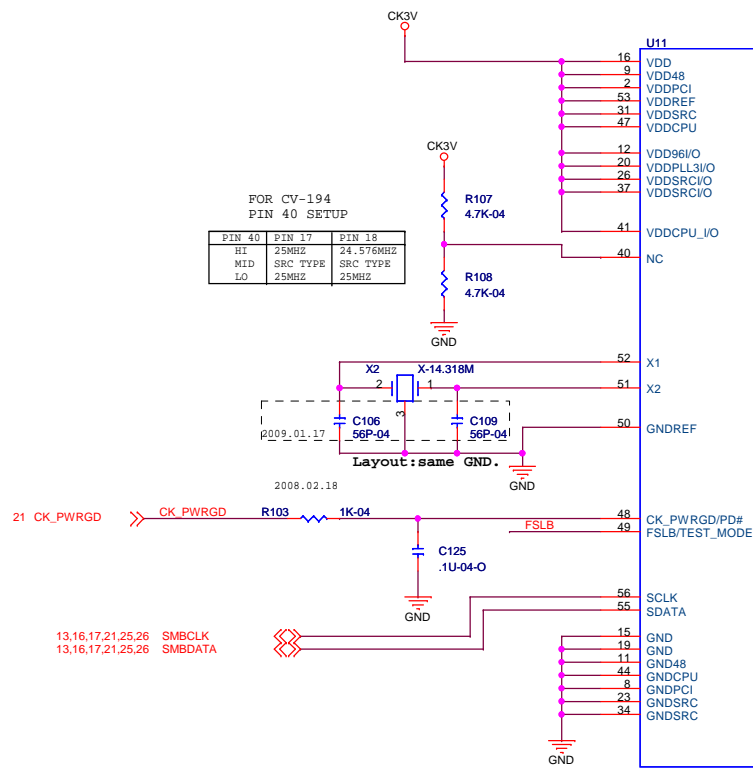
Title CPU-SOCKET LG775-3

Size Custom

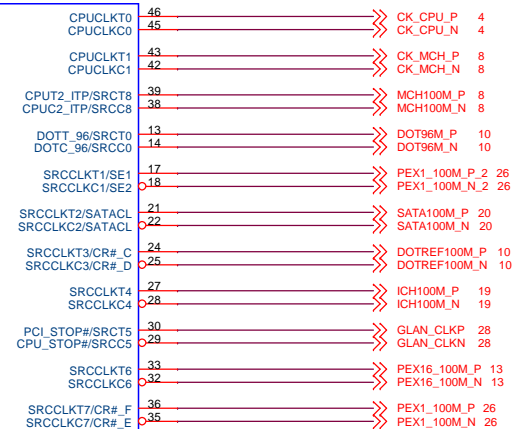
Document Number G43T-DM1

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IDTCV194BPAGS



CPU

MCH(FSB)

MCH(PCIE)

MCH(VGA) REGISTERS {BYTE1}{BIT7} SET HI

X1 - 2

ICH(SATA)

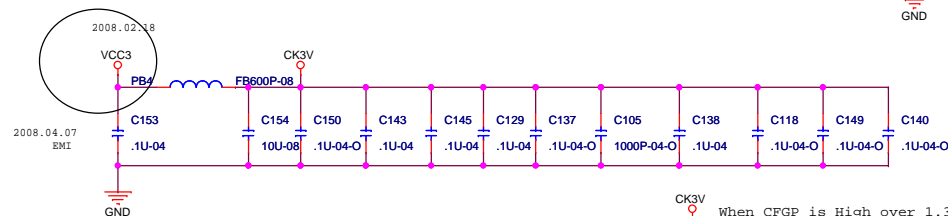
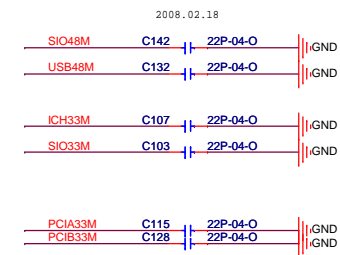
MCH(VGA)

ICH

LAN

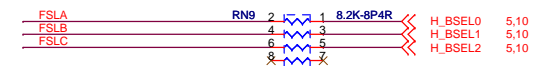
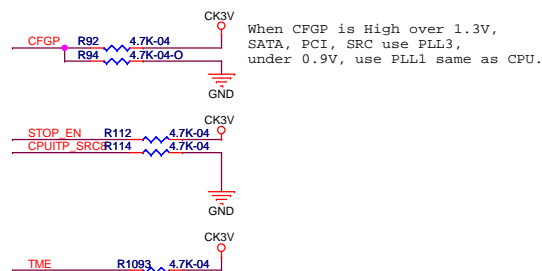
X16

X1



LO FOR PCI & CPU FUNCTION START
LO FOR SRC 100MHZ CLOCK

ENABLE INTERNAL DAMPING



Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU CLOCK (MHZ)
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00

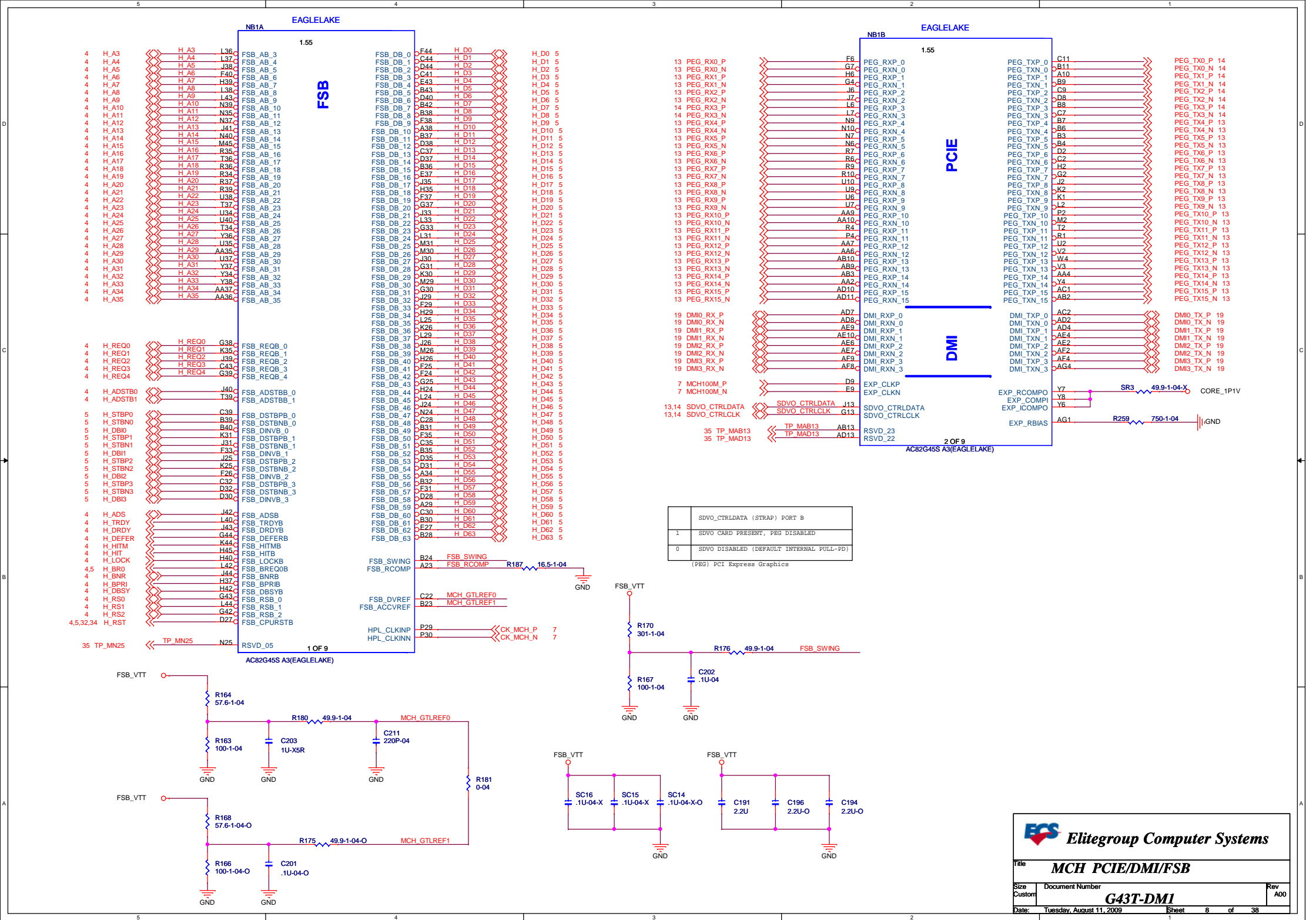
ECS Elitegroup Computer Systems

Title **CV190**

Size Custom Document Number **G43T-DM1**

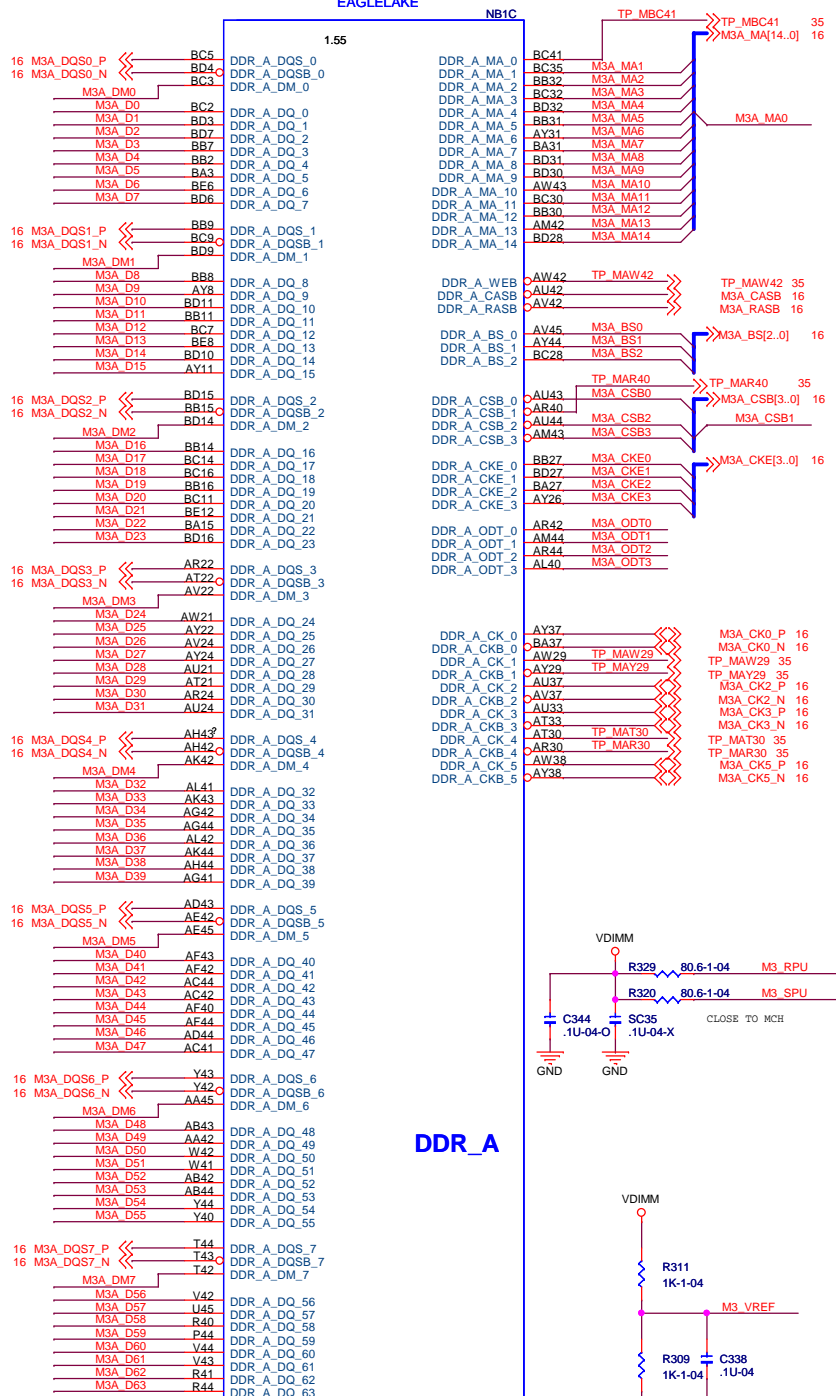
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EAGLELAKE

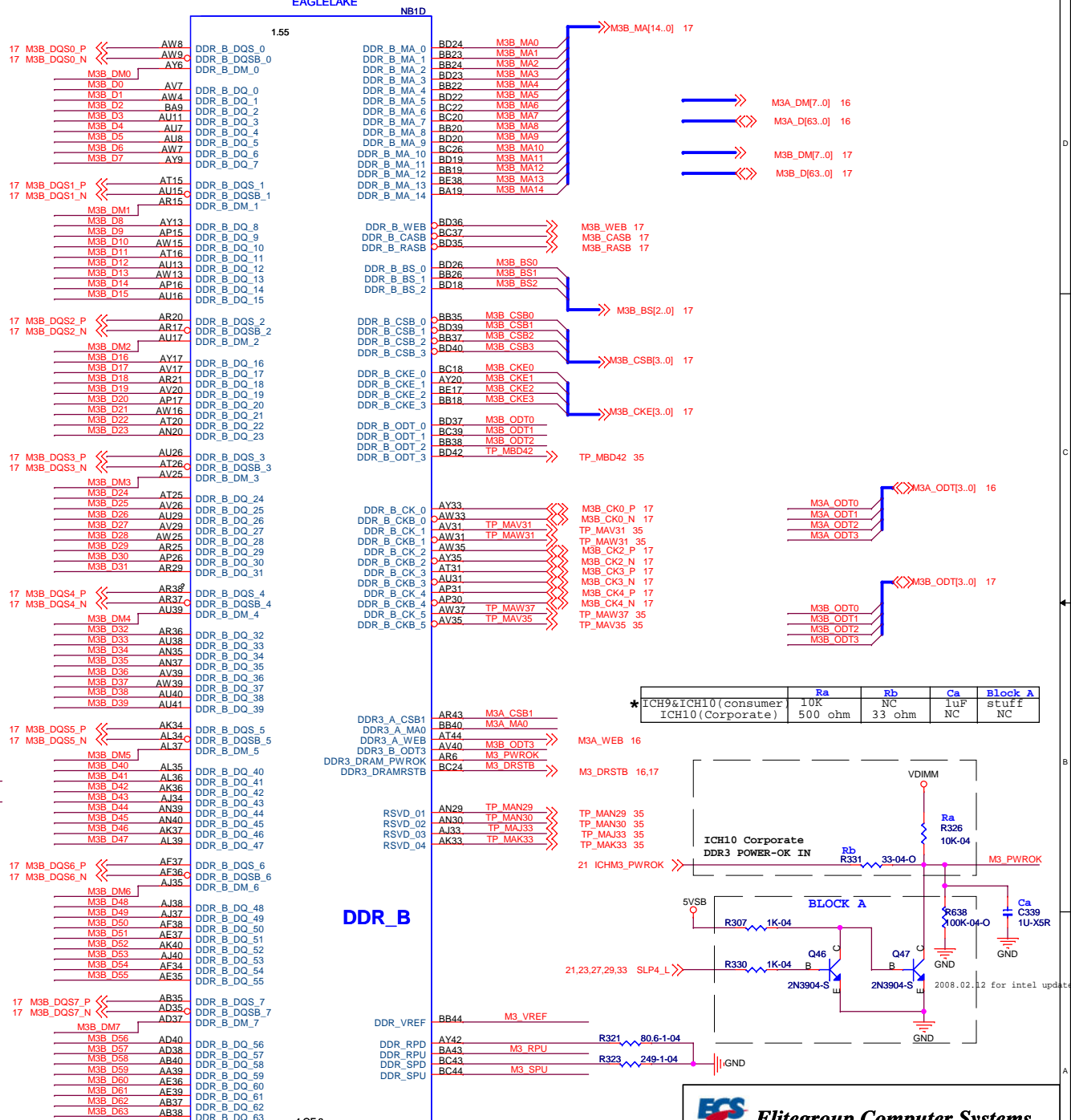
NB1C



AC82G45S A3(EAGLELAKE)

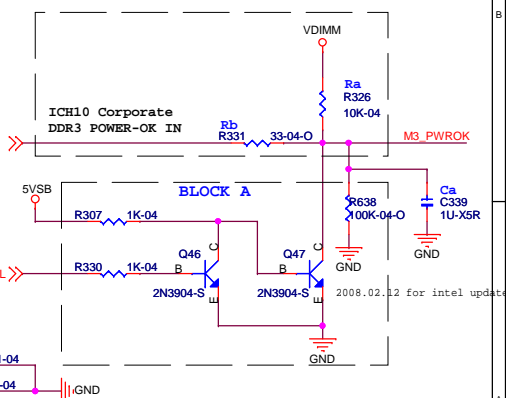
EAGLELAKE

NB1D



AC82G45S A3(EAGLELAKE)

	Ra	Rb	Ca	Block A
* ICH9&ICH10 (consumer)	10K	NC	1uF	stuff
ICH10 (Corporate)	500 ohm	33 ohm	NC	NC



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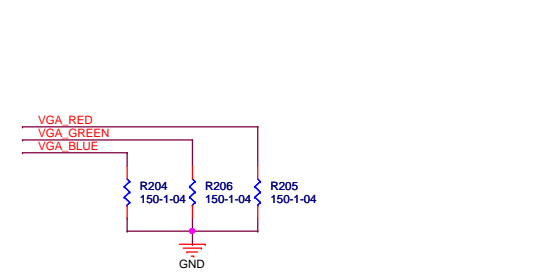
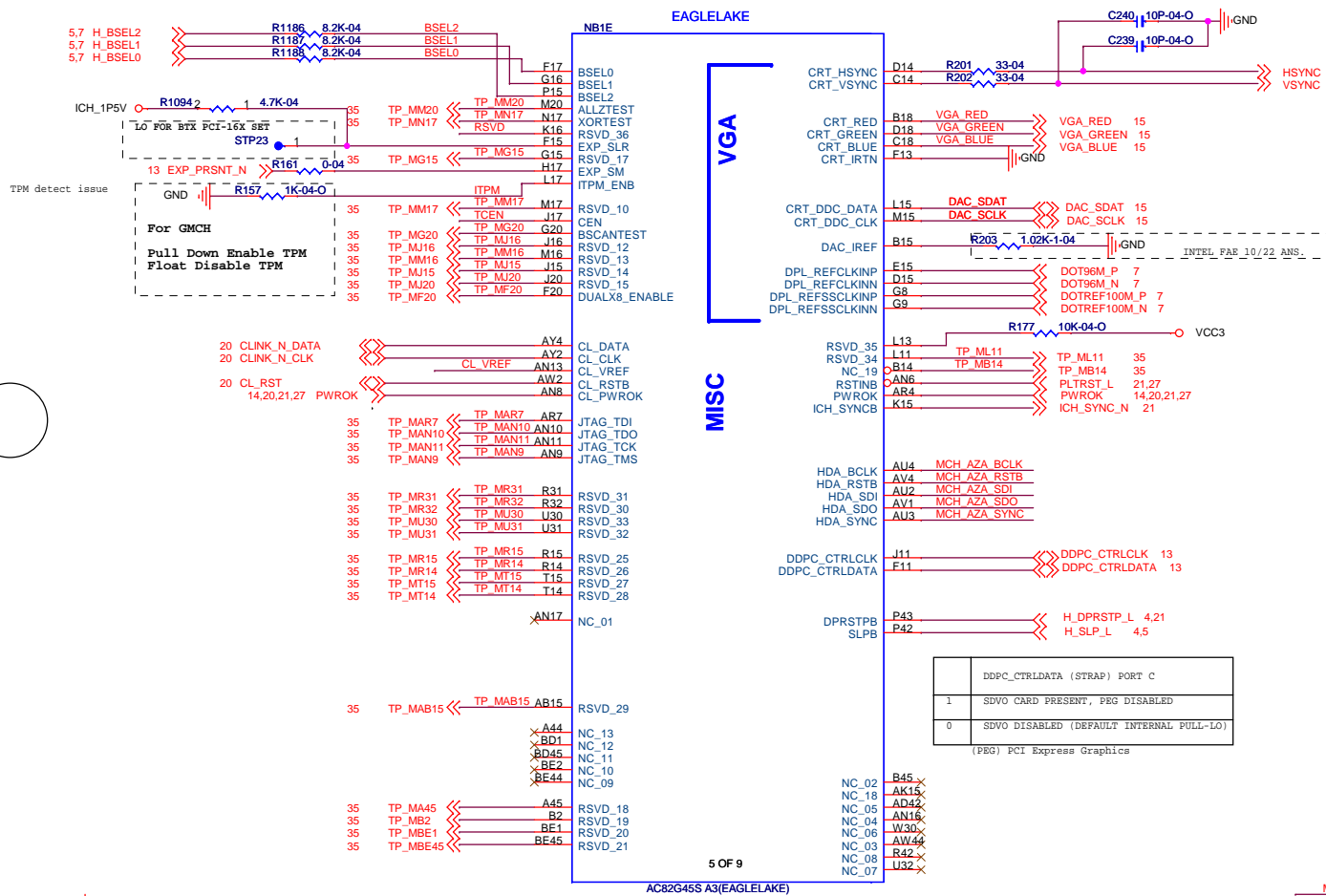
Title **MCH /DDR III 1/DDR III 2**

Size Custom Document Number

G43T-DM1

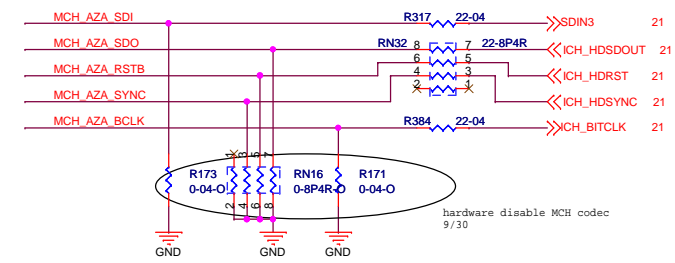
Rev A00

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DDPC_CTRLCLK (STRAP) PORT C	
1	SDVO CARD PRESENT, PEG DISABLED
0	SDVO DISABLED (DEFAULT INTERNAL PULL-LO)

(PEG) PCI Express Graphics



hardware disable MCH codec
9/30

Intel Integrated TPM Straps

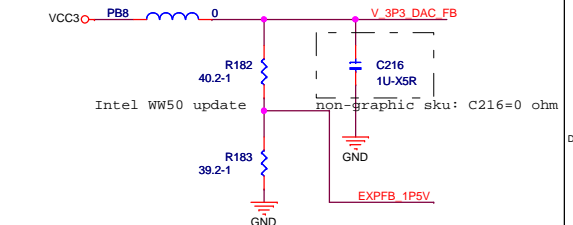
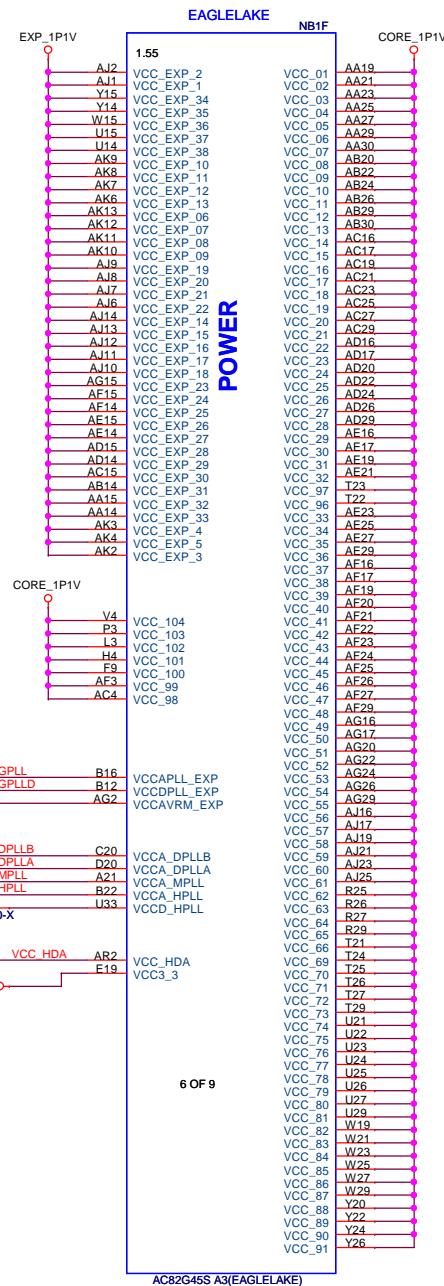
	ICH 10,C12 pin	ICH 10,C26 pin	MCH,L17 pin
Disable	Pulldown	Float	Float
Enable	Pullhi	Pullhi	Pulldown

For TLS confidentiality, a HW strap is provided on MCH. For platforms that support Intel AMT, TCEN is enabled by default. For platforms that do not support Intel AMT, no action is needed. For platforms that support Intel AMT but do not want to enable TLS confidentiality, TCEN can be disabled using the mechanism described below. TCEN signal is connected to pin J17 of the Intel® 4 Series Chipset. TCEN is enabled by default with the pull-down resistor site emptied. Populating a 1k ohm pull-down resistor disables TLS Confidentiality. For additional information on TLS confidentiality options available for Intel® AMT, please refer to the Intel AMT Product Requirements Document.

STUFF (R) FOR NON AMT & NON-CORWIN SPRING

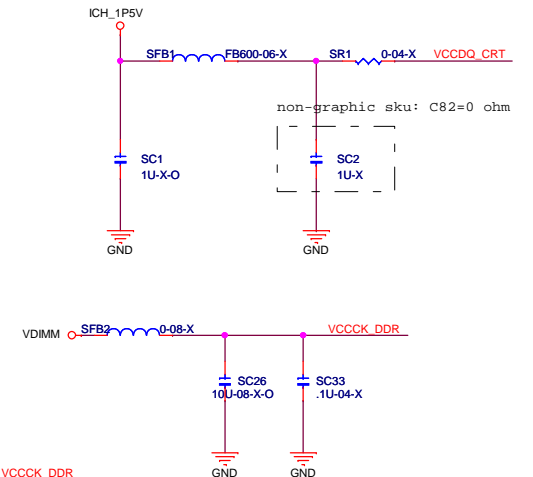
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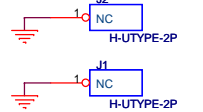
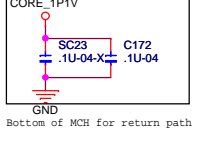
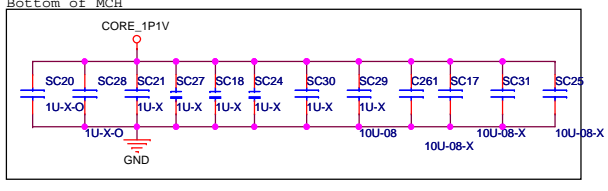
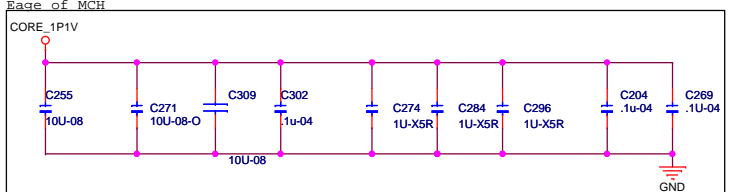
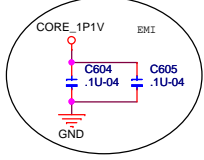
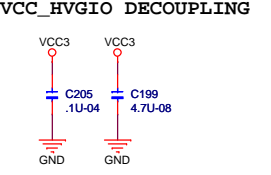
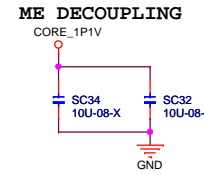
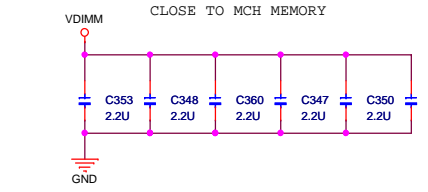
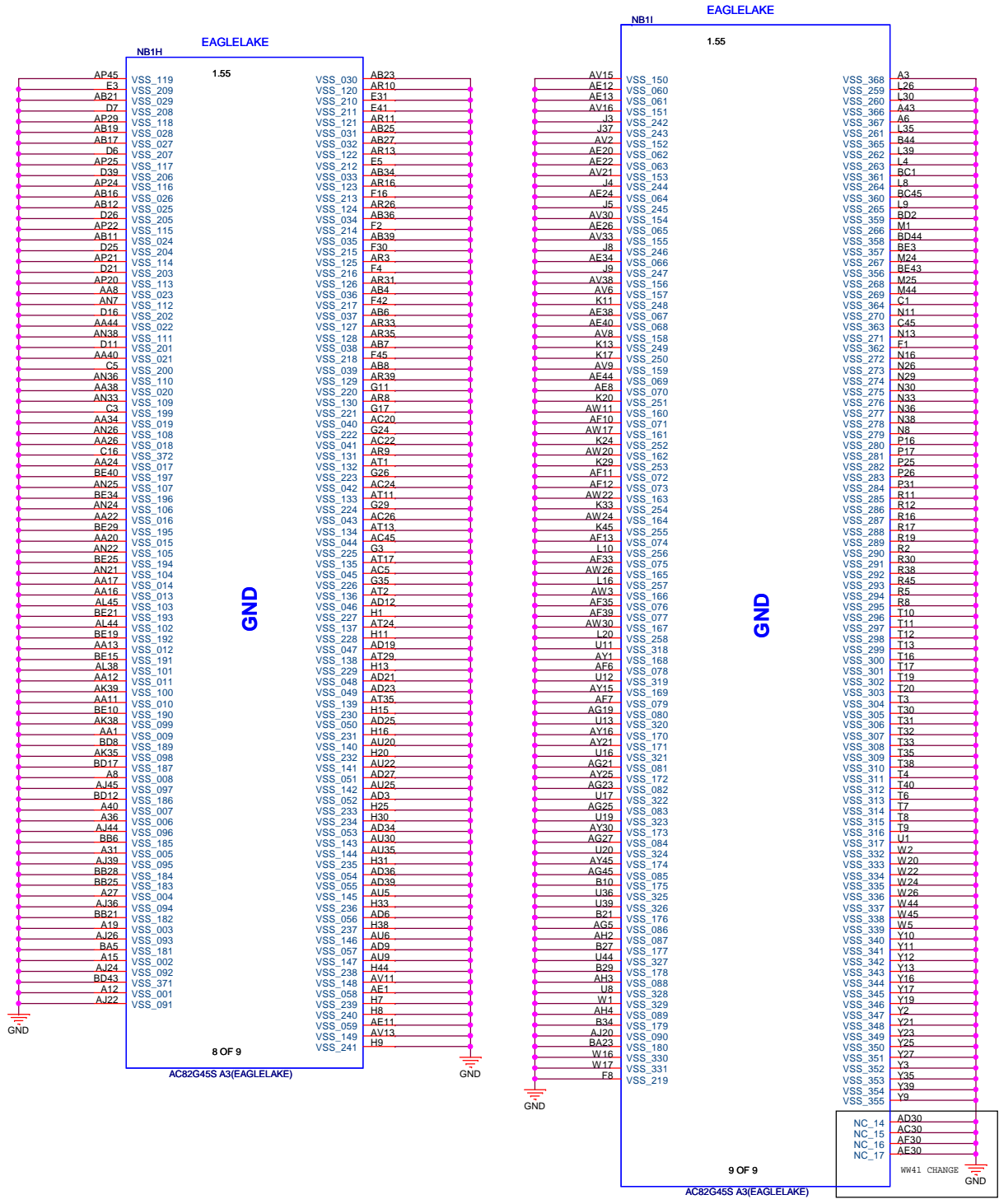
Title MCH /VGA/MISC		
Size Custom	Document Number G43T-DM1	Rev A00
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EAGLELAKE SQU TYPE	
Q SQU	RE==NC
G SQU	RE==NC
P SQU	RE==0 ohm

* Intel WW43 UPDATA





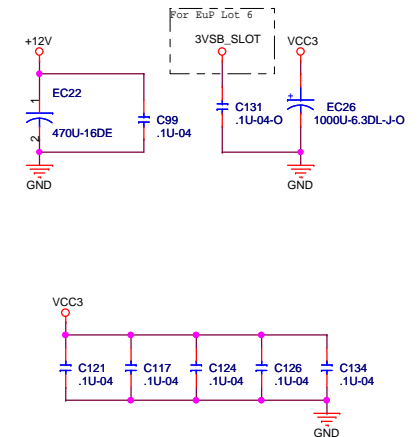
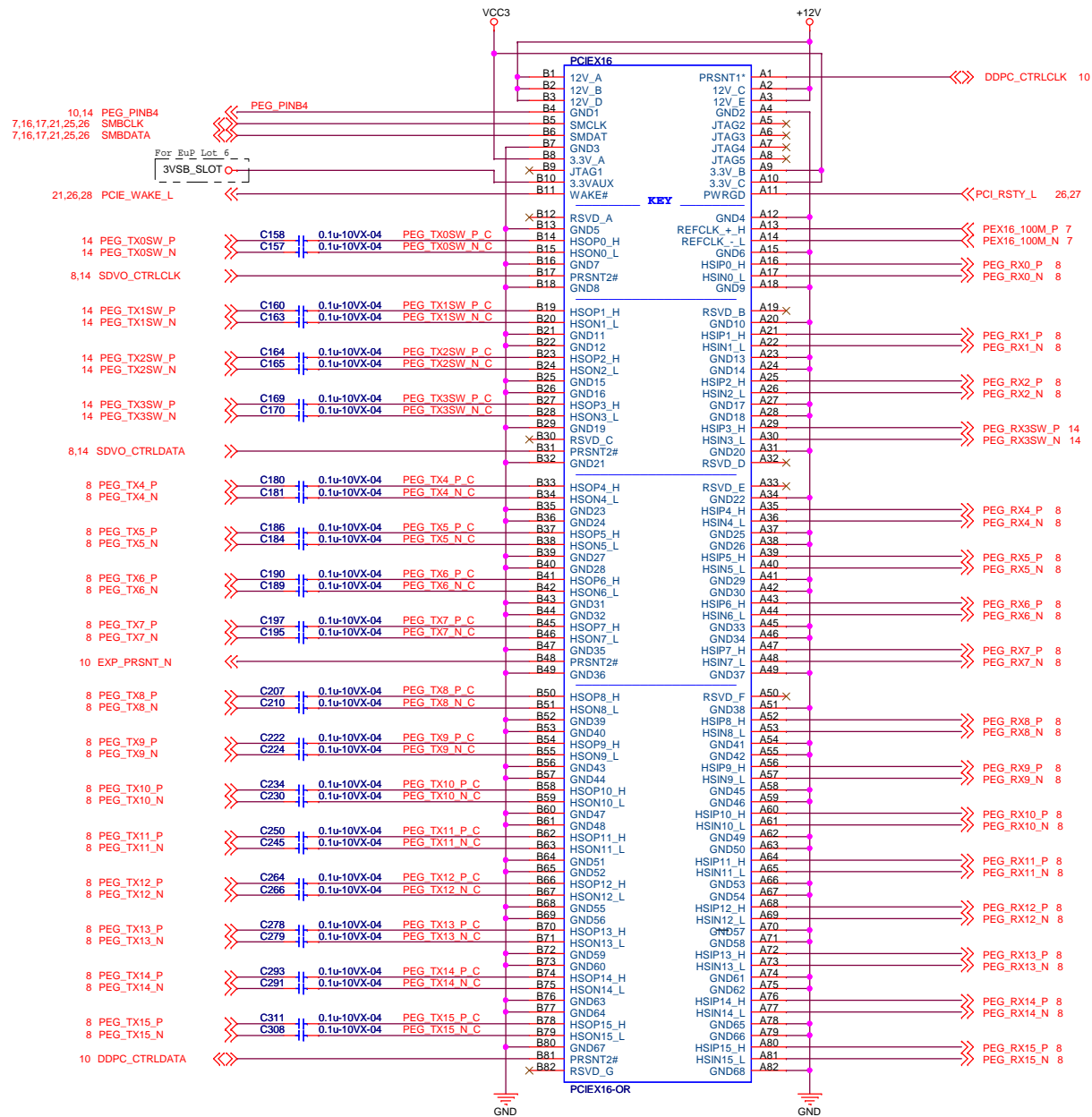
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Title: **MCH /GND**

Size: Document Number **G43T-DM1** Rev: A00

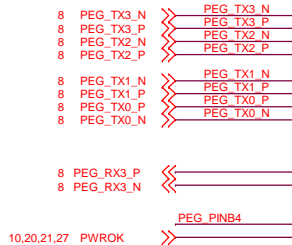
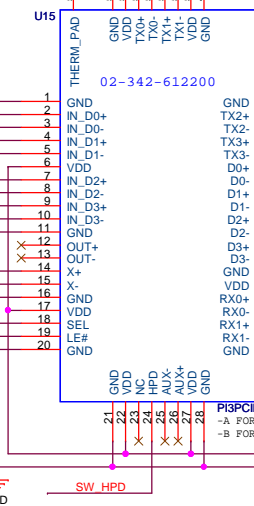
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Date: Tuesday, August 11, 2009 Sheet 12 of 38

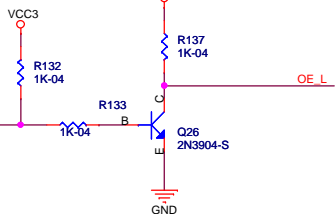


SW_SEL	Function
Hi	HDMI mode
Lo	PCIEx16 mode

Switch

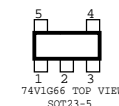


10,20,21,27 PWROK



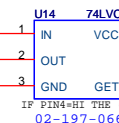
10,13 PEG_PINB4

8,13 SDVO_CTRLCLK

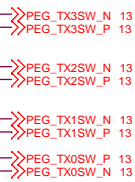


74V1G66 TOP VIEW
SOT23-5

8,13 SDVO_CTRLDATA

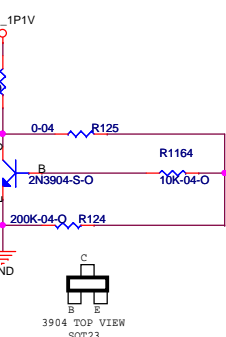
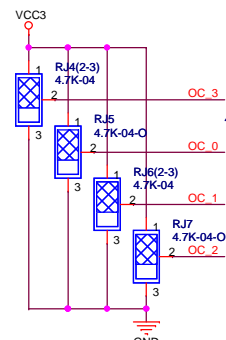


74V1G66 TOP VIEW
SOT23-5



SW_CLK_N
SW_CLK_P
DATA0_N
DATA0_P
DATA1_N
DATA1_P
DATA2_N
DATA2_P

DDC_EN	Passgate
3.3V	Enable
0	Disable

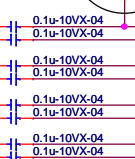


3904 TOP VIEW
SOT23

Level shifter noise issue

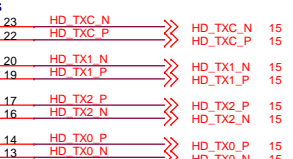
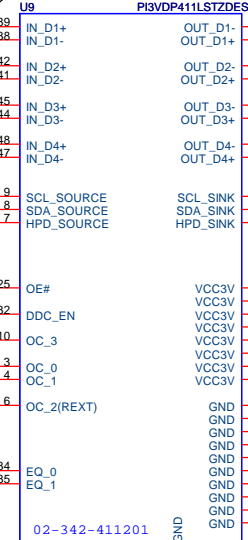
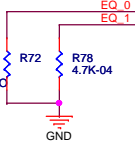
9/30

Level Shifter



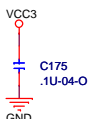
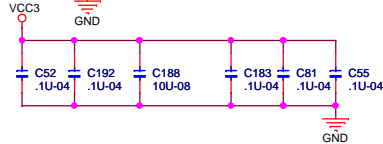
SHD_CLK
SHD_DATA
HPD
3.3V level

OE_L
PEG_PINB4
OC_3
OC_0
OC_1
OC_2



HD_HPDP	Status
Hi	Plugged
Lo	unplugged

HD_HPDP:Internal 100K pull low



OC_3	OC_2	OC_1	OC_0	Vswing (mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0

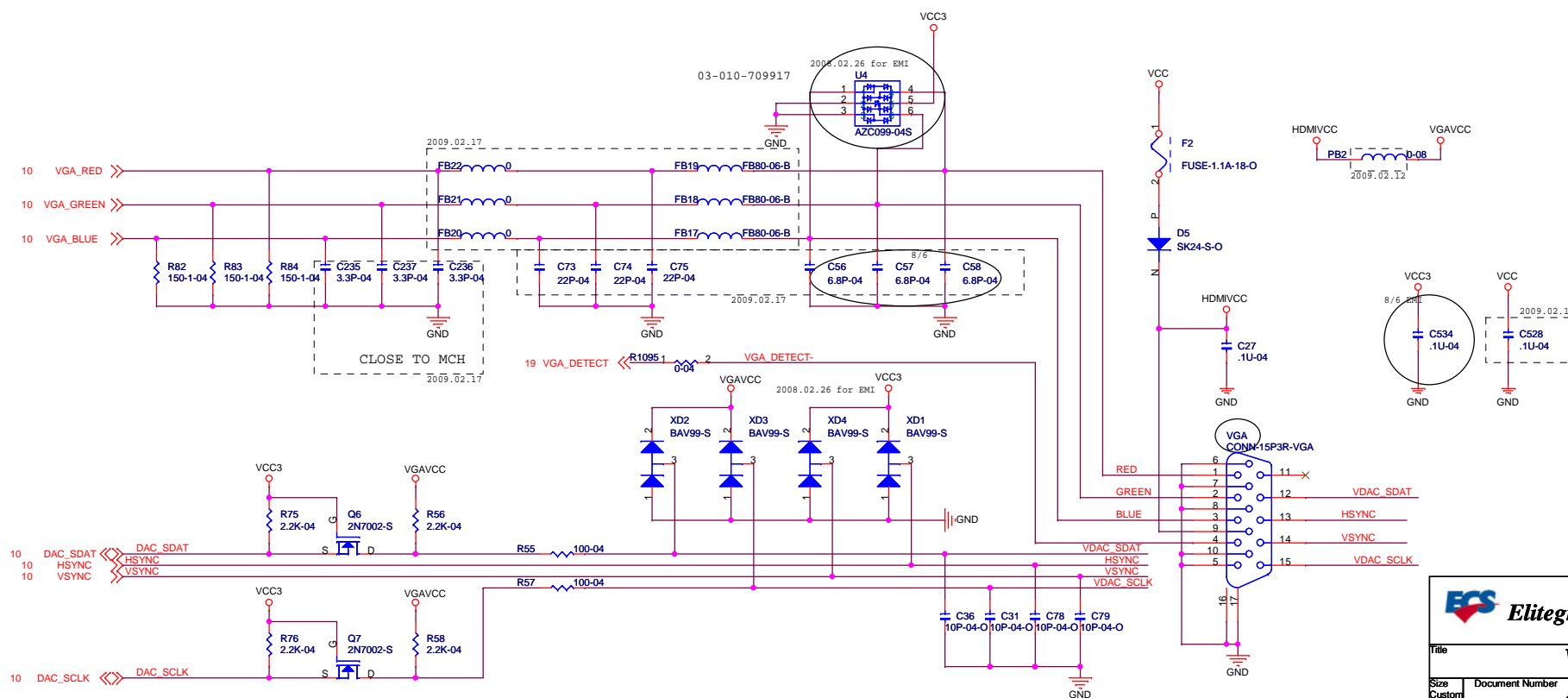
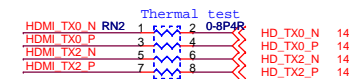
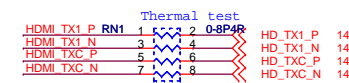
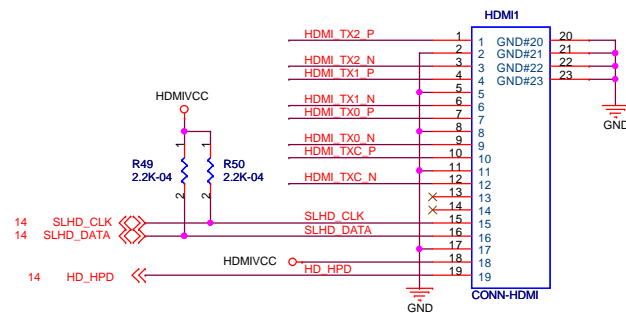
EQ_0	EQ_1	Equalization(dB)
0	0	3
0	1	7.2
1	1	20

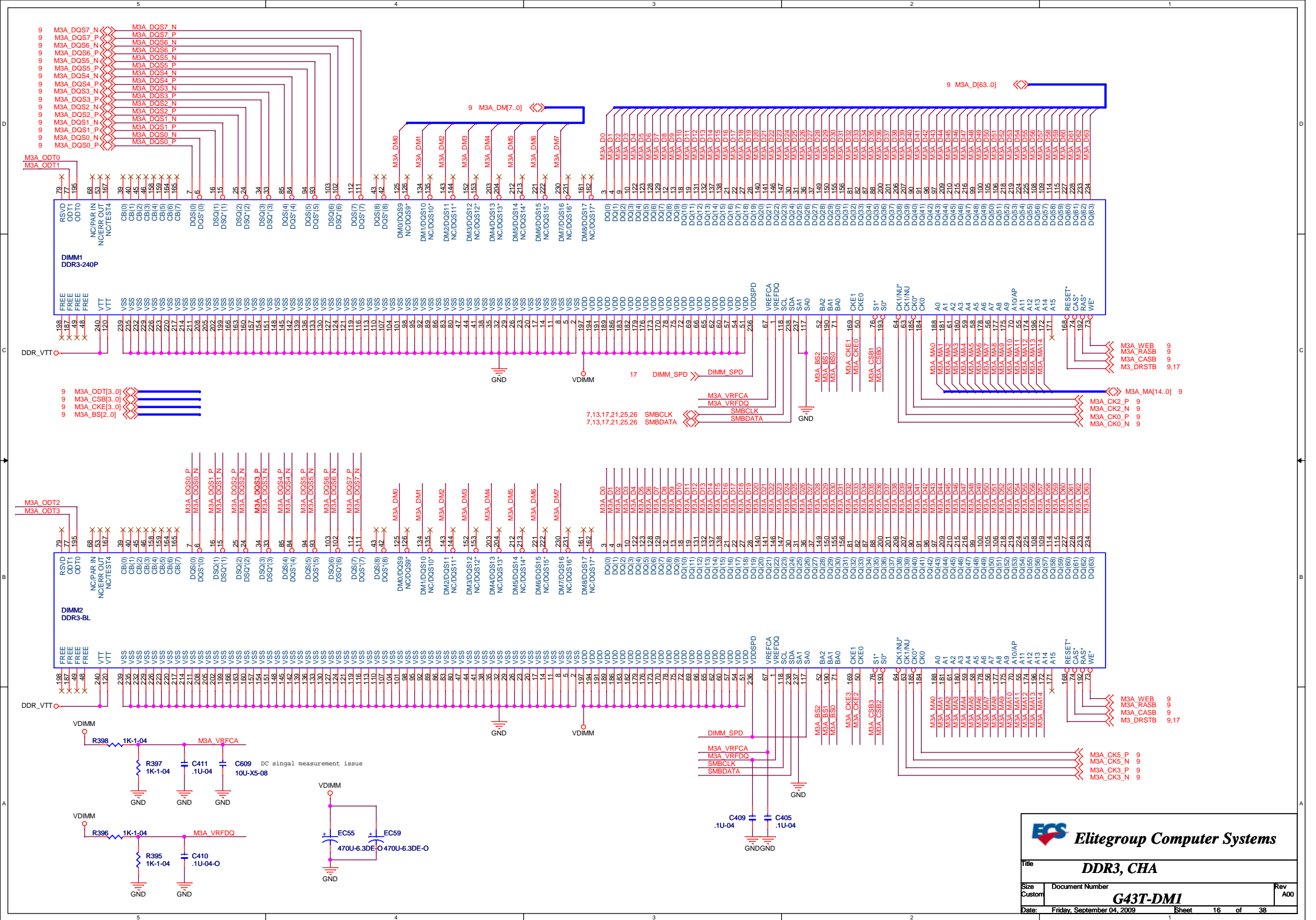
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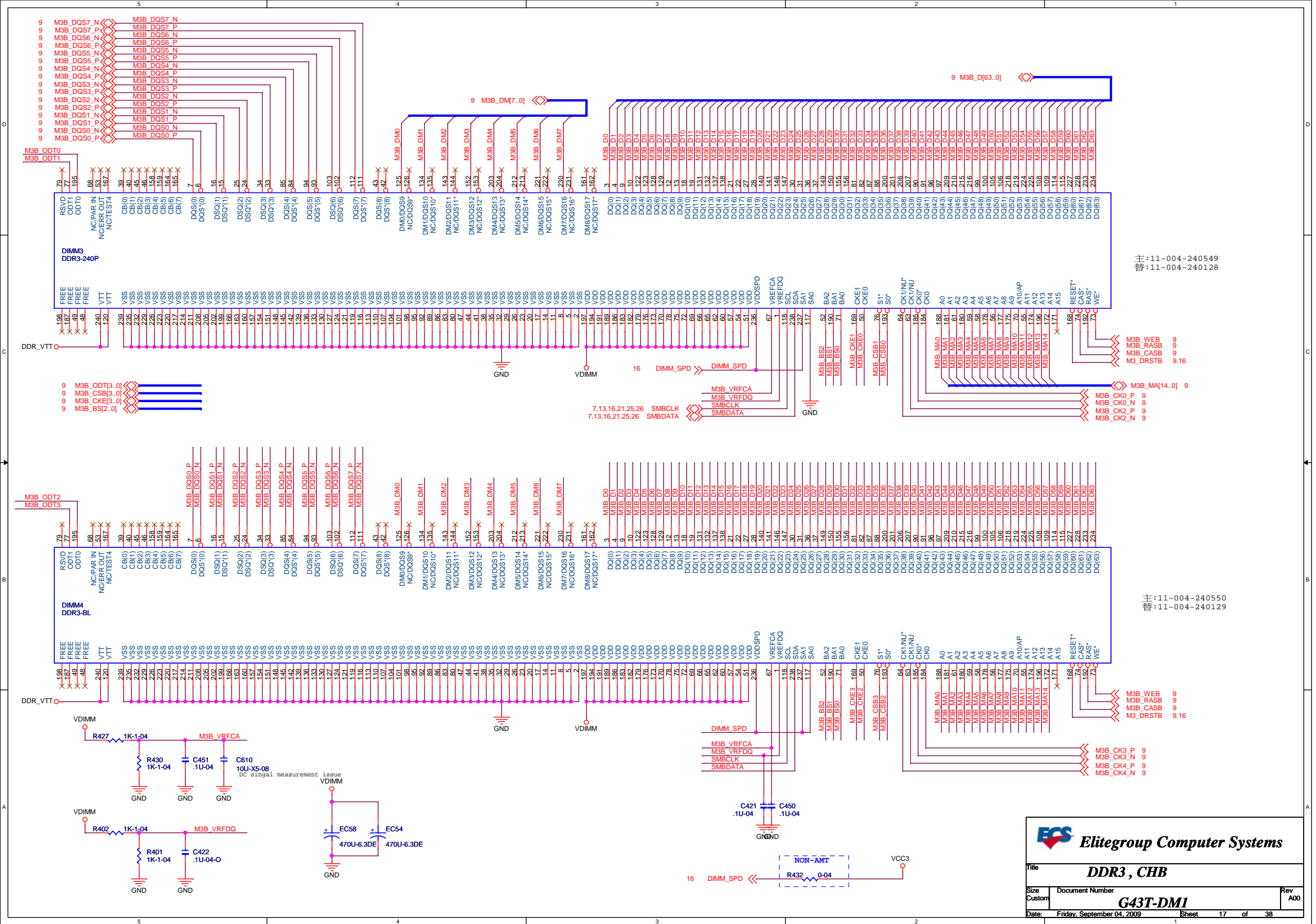
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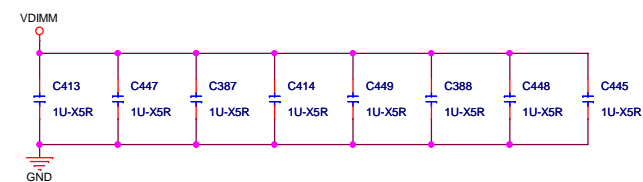
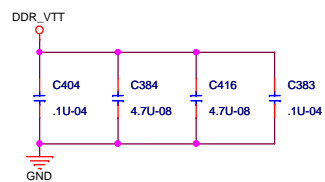
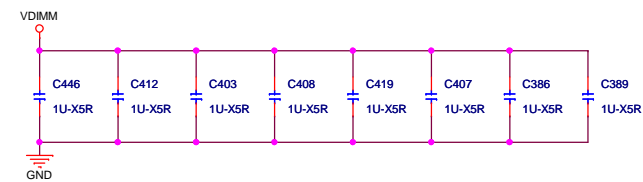
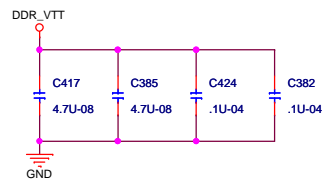
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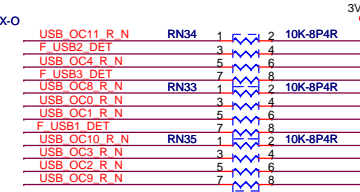
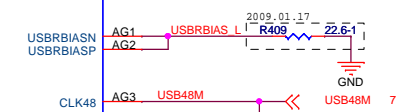
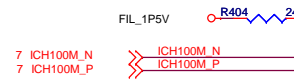
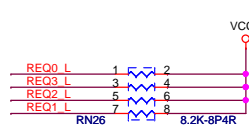
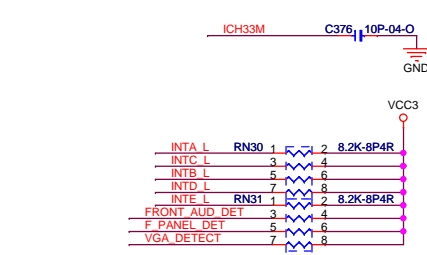
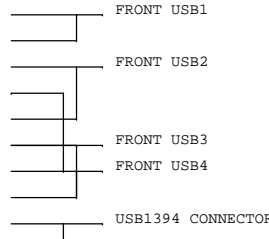
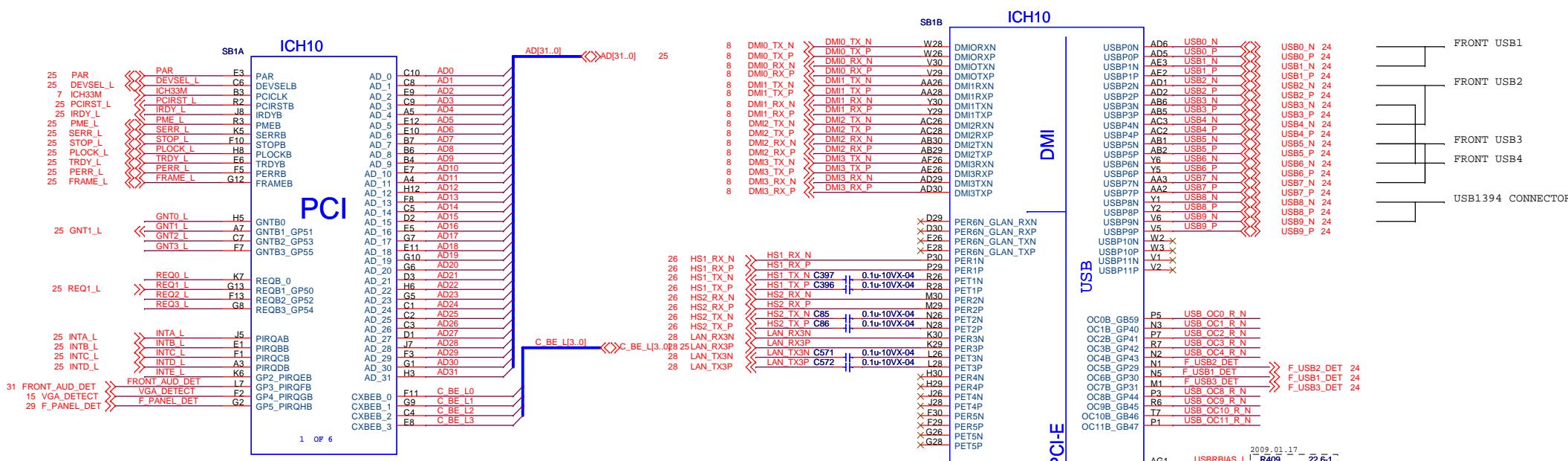
Date: Monday, September 14, 2009 Sheet 14 of 38









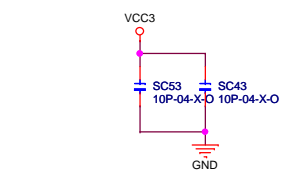
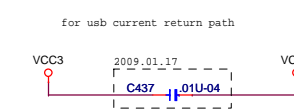


for usb current return path

GNT1_L:ES1 compatible mode is for server platforms only
this signal should not be pulled low for desktop and mobile
internal pull-up


GNT2_L:This signal has a weak internal pull-up
Sets bit 2 of RPC.PC2(Chipset config registers:offset 0224h)when sampled low

GNT3_L:this indicates the the system is strapped to the "top-block" swap mode
Internal pull-up This signal should not be pulled low unless using XOR chain testing



BOOT BIOS DESTINATION SELECTION		
GNT0_L	SPI_CS1	BOOT BIOS DESTINATION
0	1	SPI
1	0	PCI
1	1	LPC
0	0	Reserved

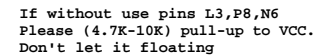
*Default

**Elitegroup Computer Systems**

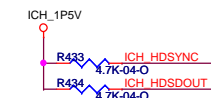
Title**ICH9/10 PCI/PCI-E**

Size CustomDocument Number**G43T-DM1**Rev A00

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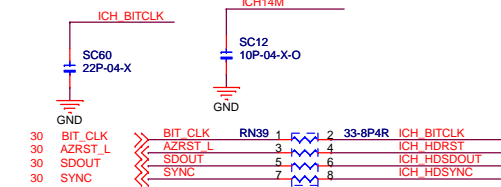


	ICH 10,C12 pin	ICH 10,C26 pin	MCH,L17 pin
Disable	Pulldown	Float	Float
Enable	Pullhi	Pullhi	Pulldown

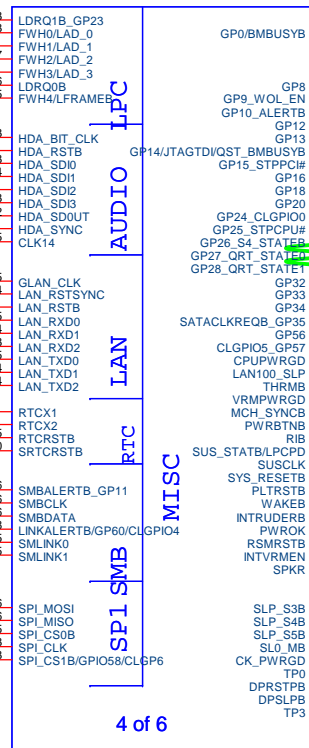
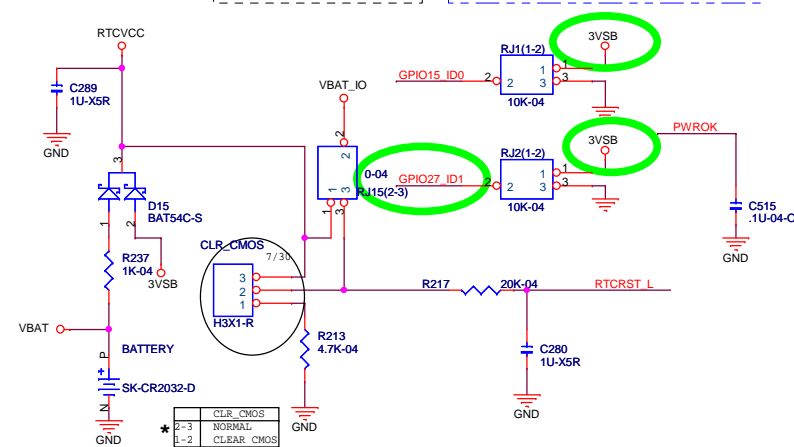
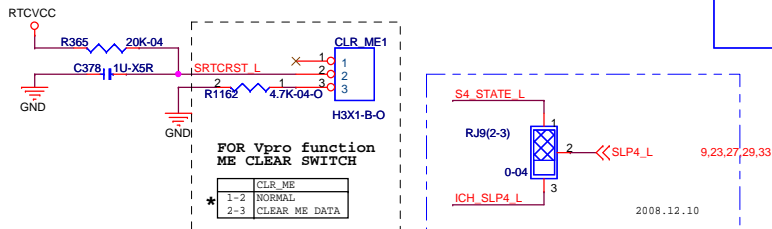


IF NOT USE GLAN THE E14 PIN
NEED 8.2K-10K PULL-DOWN

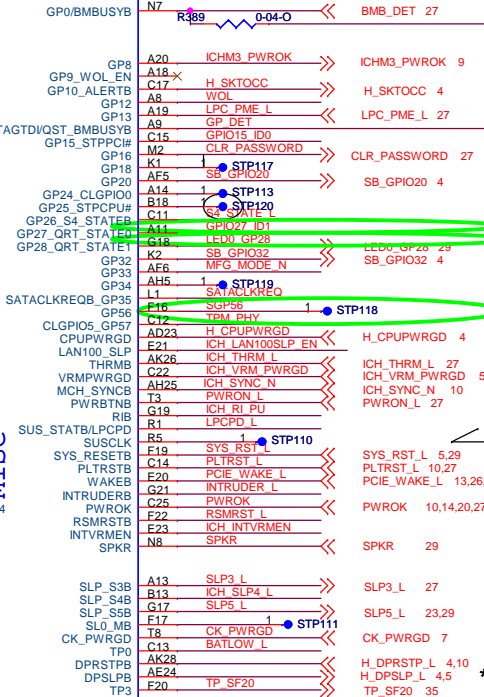
IF NOT USE INTEL LAN, THE C21 PIN
TIE TO GND



PULL-UP ENABLE TPM VCC3
FOR ICH
FLOAT DISABLE TPM R380 1K-0



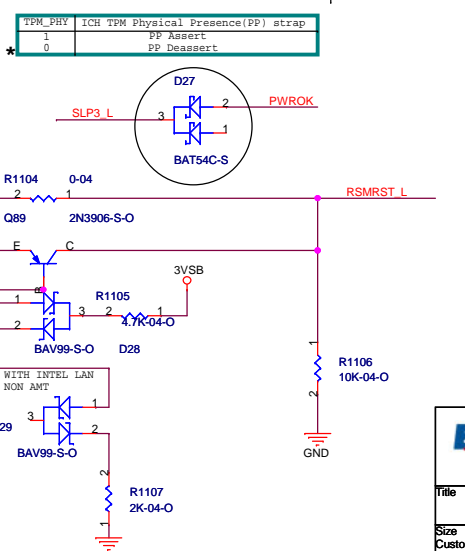
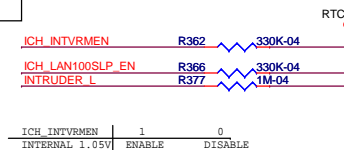
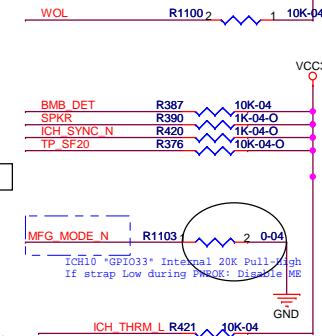
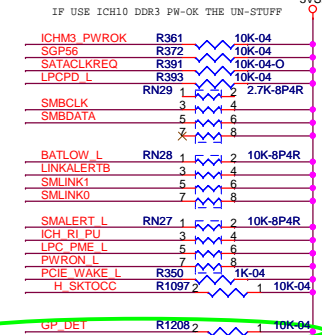
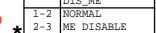
When using Intel® QST as the fan speed control -
BM_BUSY# must be connected to QST_BMBUSY
This applies to ICH10-consumer based platform only

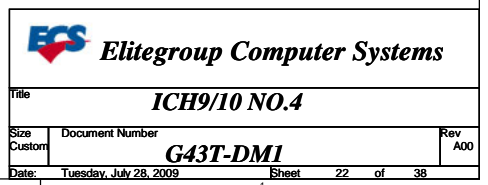


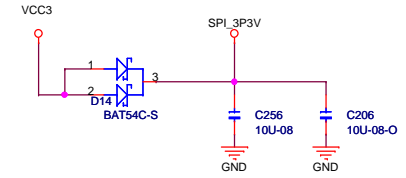
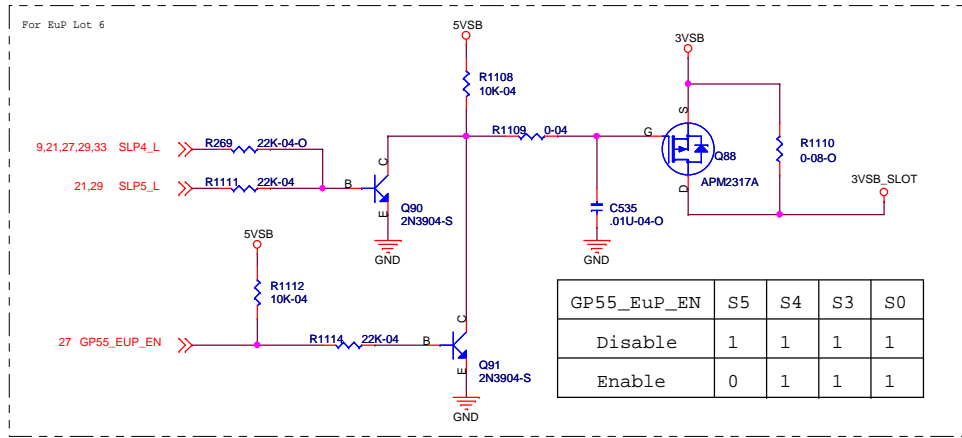
NEED COVER "GND"

For EuP Lot 6

FOR Vpro function
ME DISABLE SWITCH





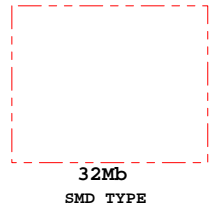
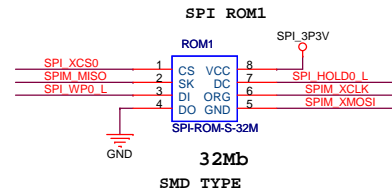
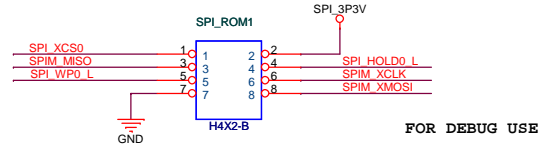
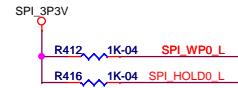
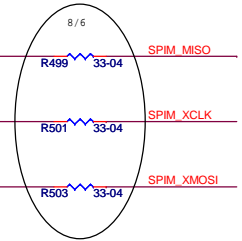


21 SPI_XCS0 >> SPI_XCS0

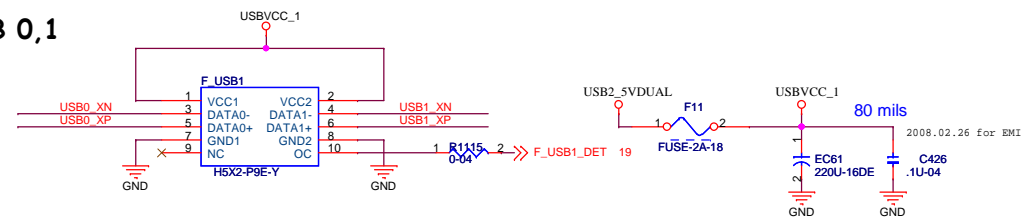
21 SPI_MISO << SPI_MISO

21 SPI_XCLK >> SPI_XCLK

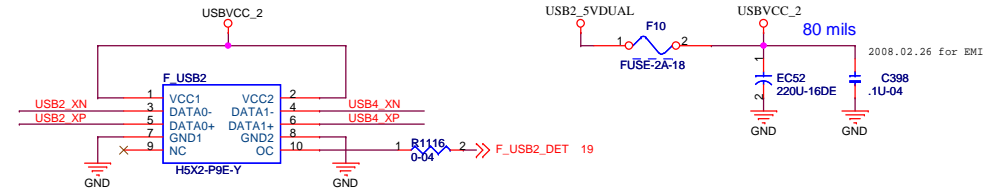
21 SPI_XMOSI >> SPI_XMOSI



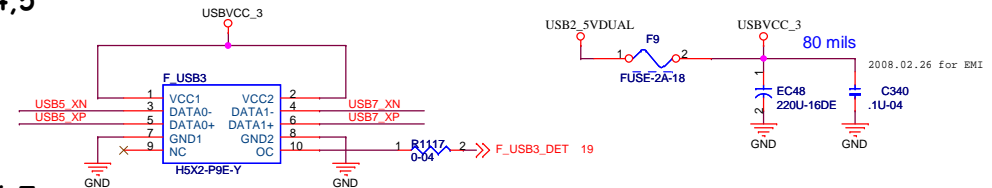
USB 0,1



USB 2,3



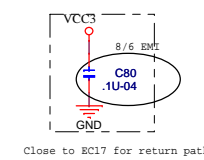
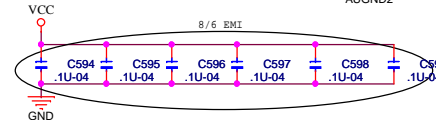
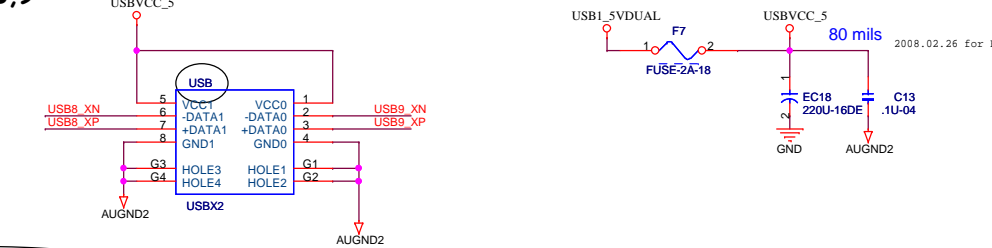
USB 4,5

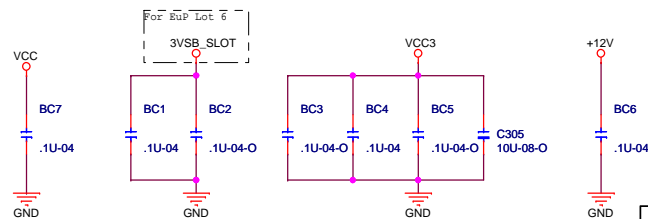
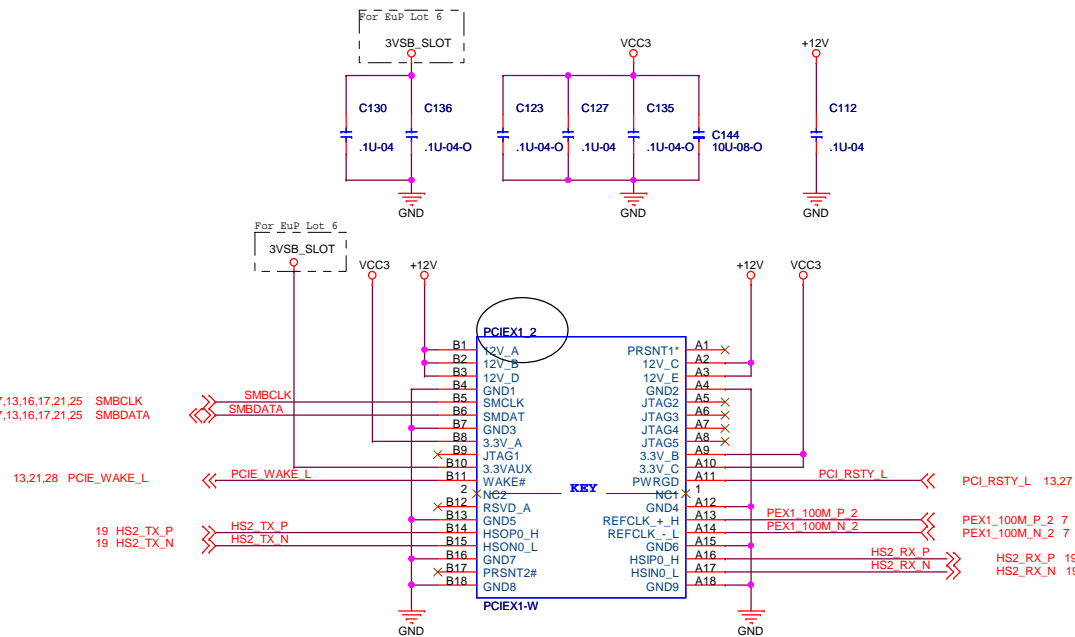
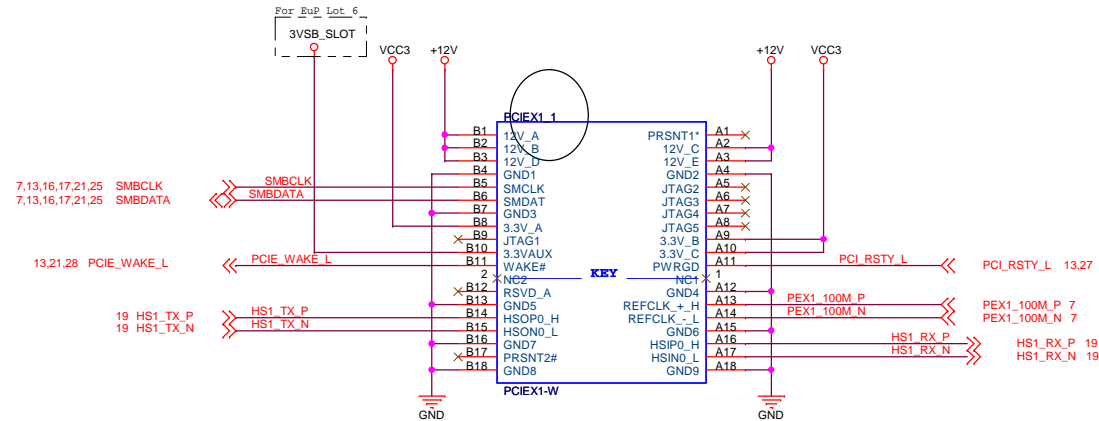
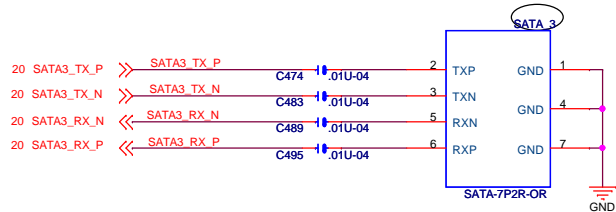
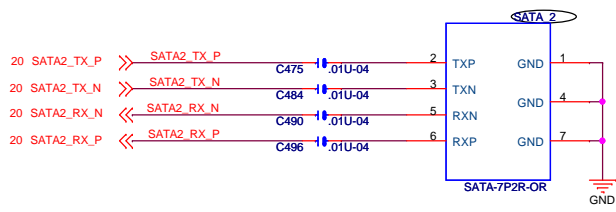
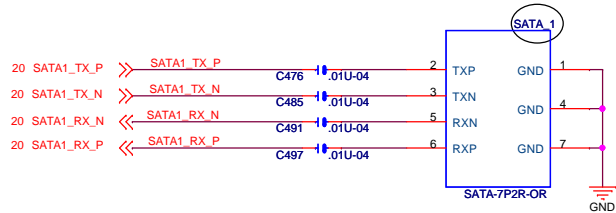
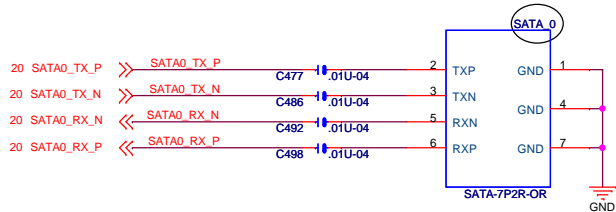


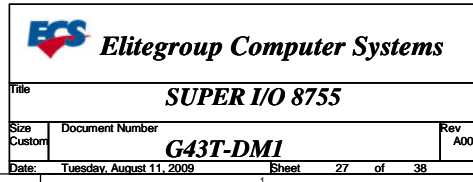
USB 6,7

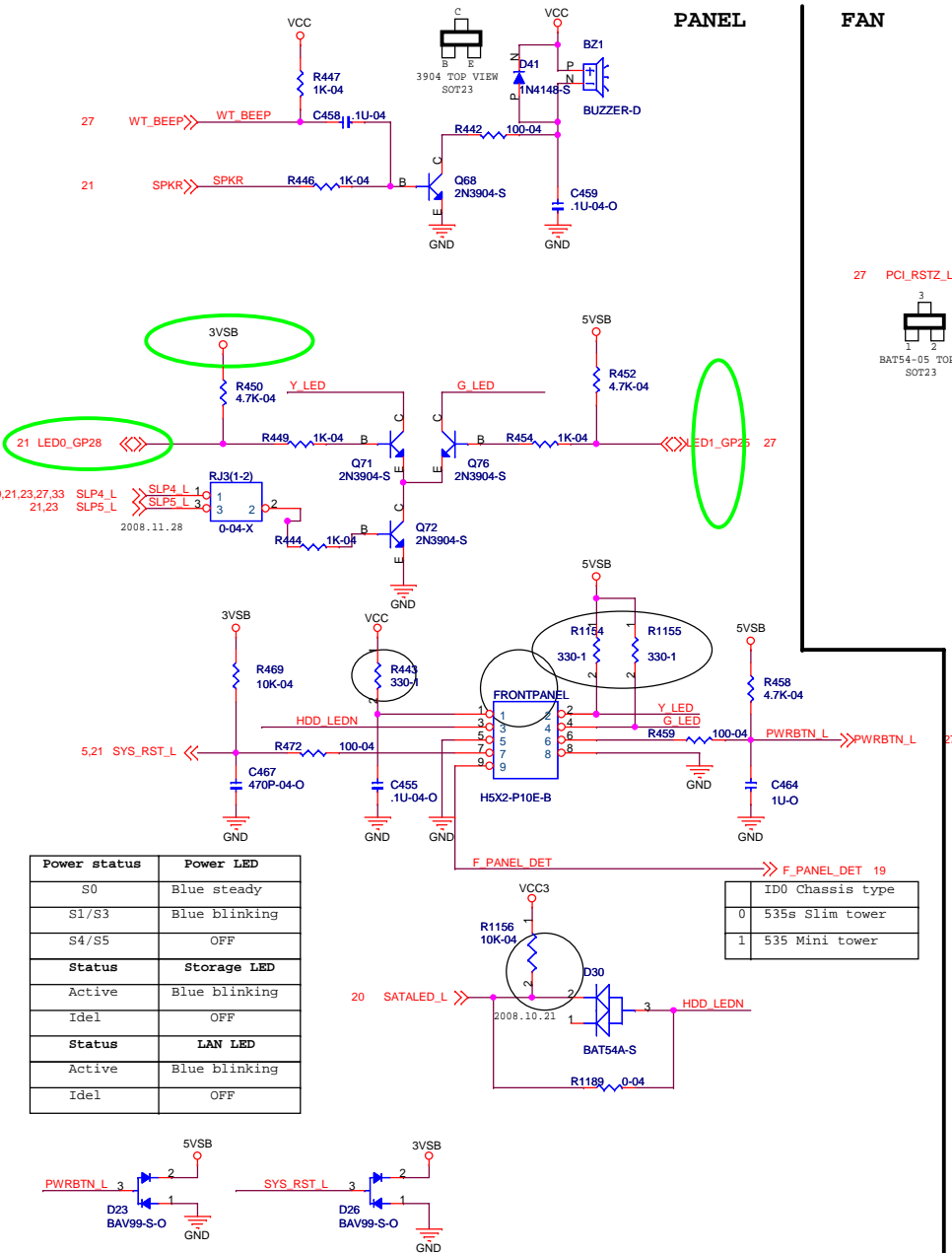


USB 8,9

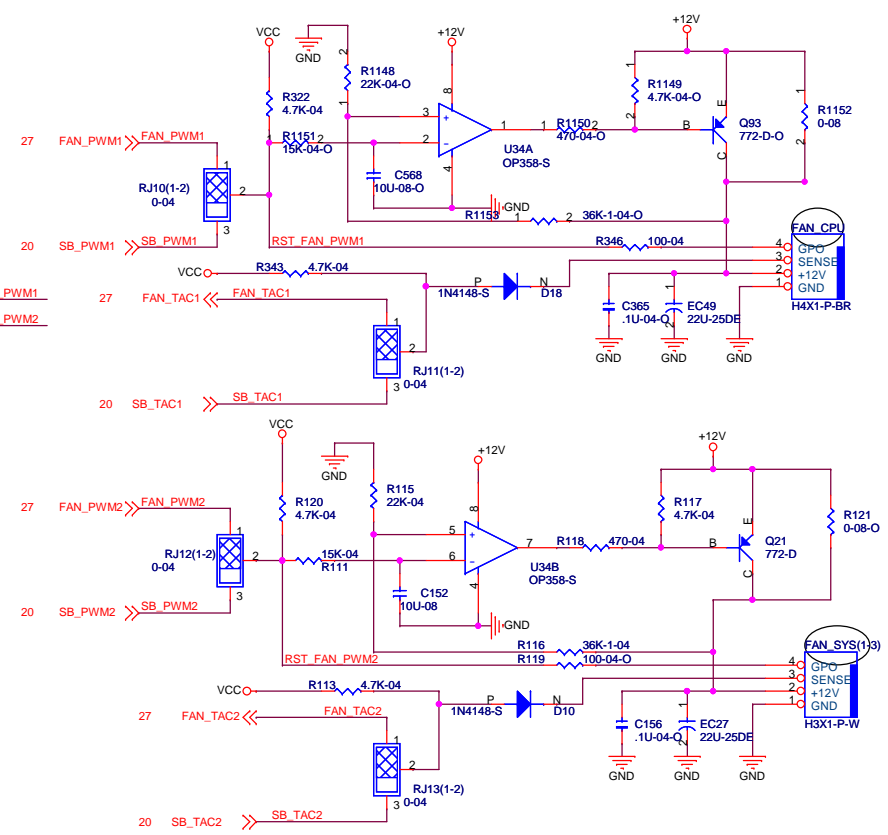
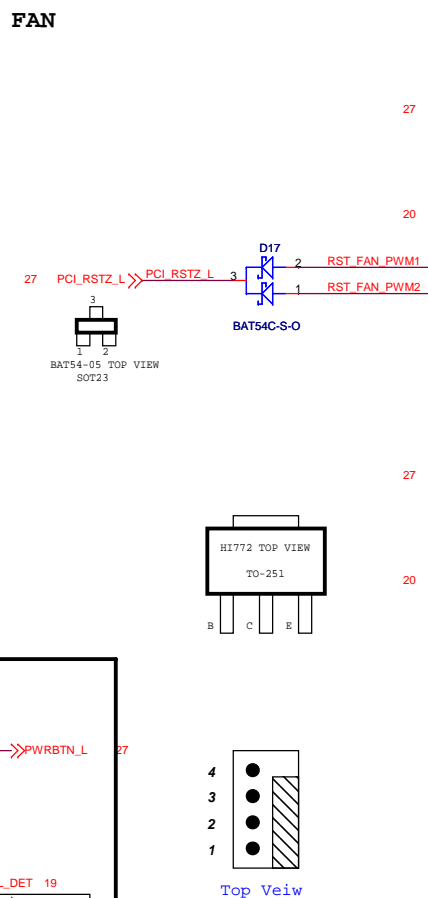








Power status	Power LED
S0	Blue steady
S1/S3	Blue blinking
S4/S5	OFF
Status	Storage LED
Active	Blue blinking
Idle	OFF
Status	LAN LED
Active	Blue blinking
Idle	OFF



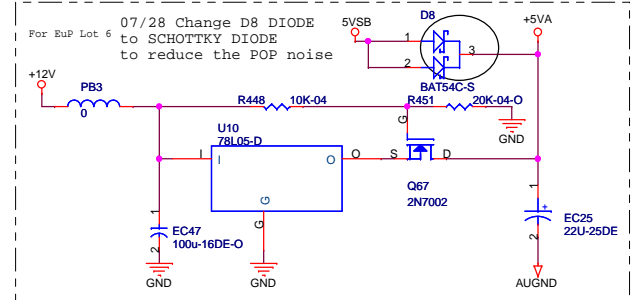
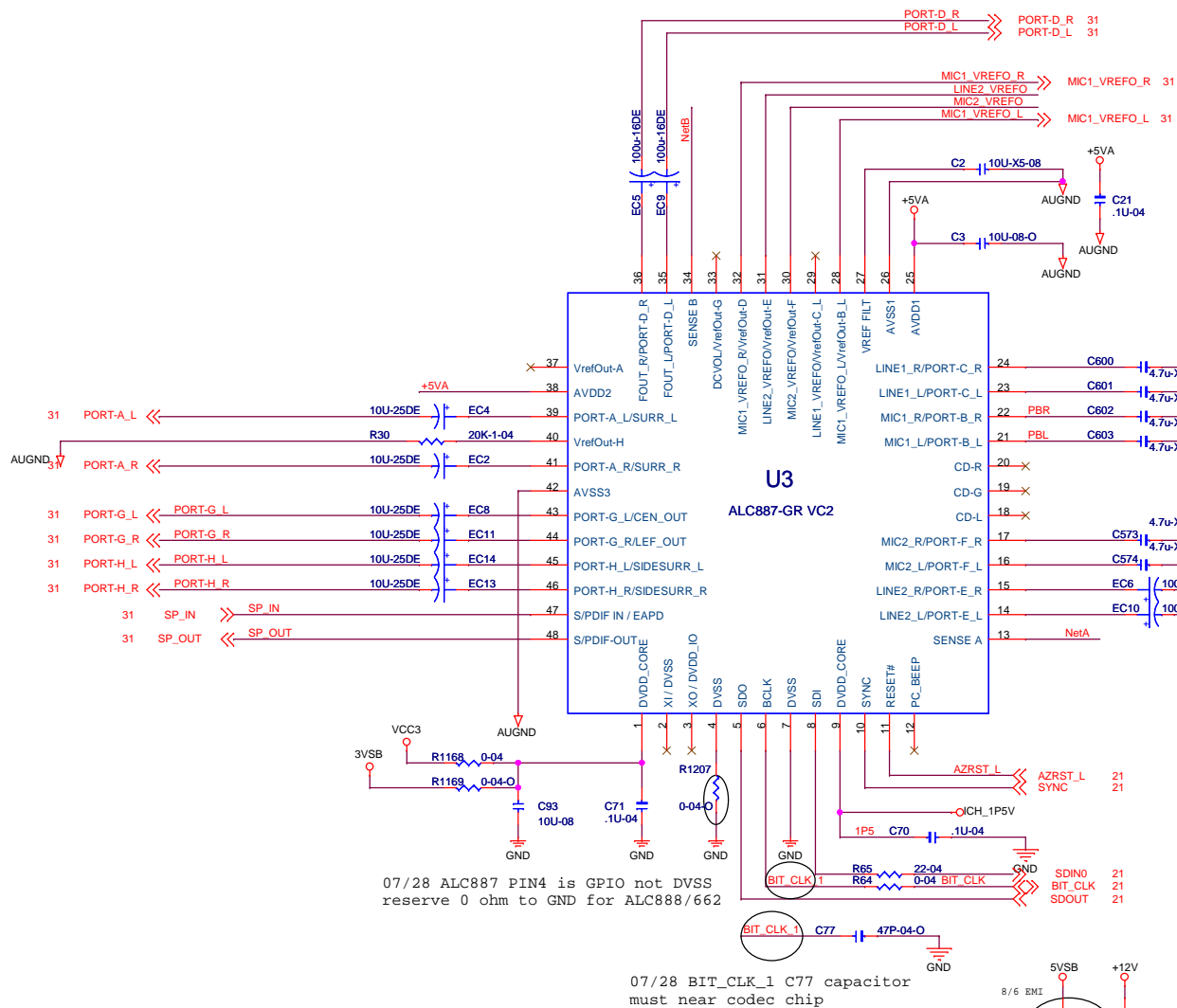
BACKUP FROM SIO GPIO

Elitegroup Computer Systems

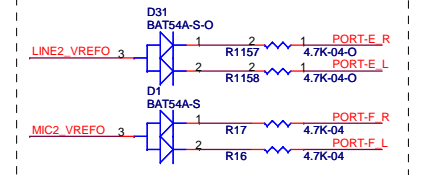
Title: **PANEL & FAN**

Size: Custom Document Number: **G43T-DM1** Rev: A00

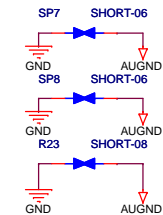
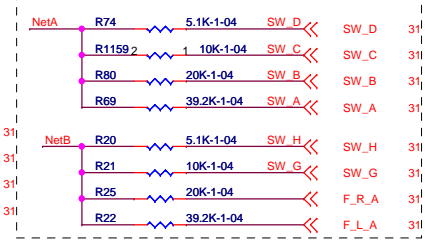
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Place near Chip



Resistors Networks

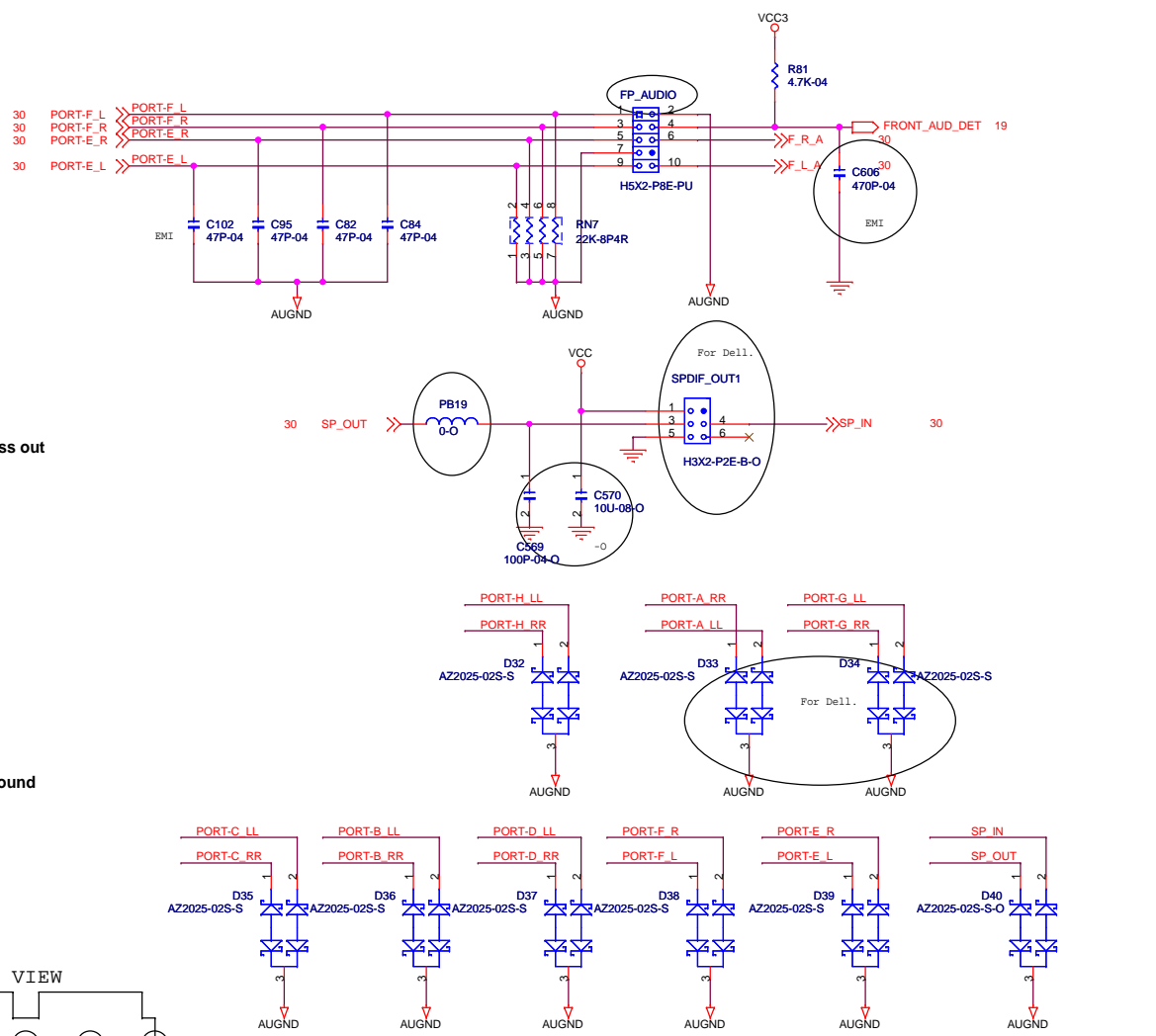
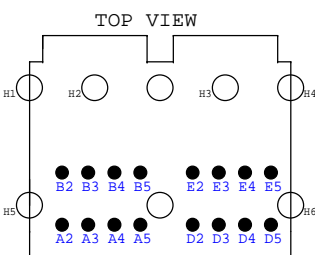
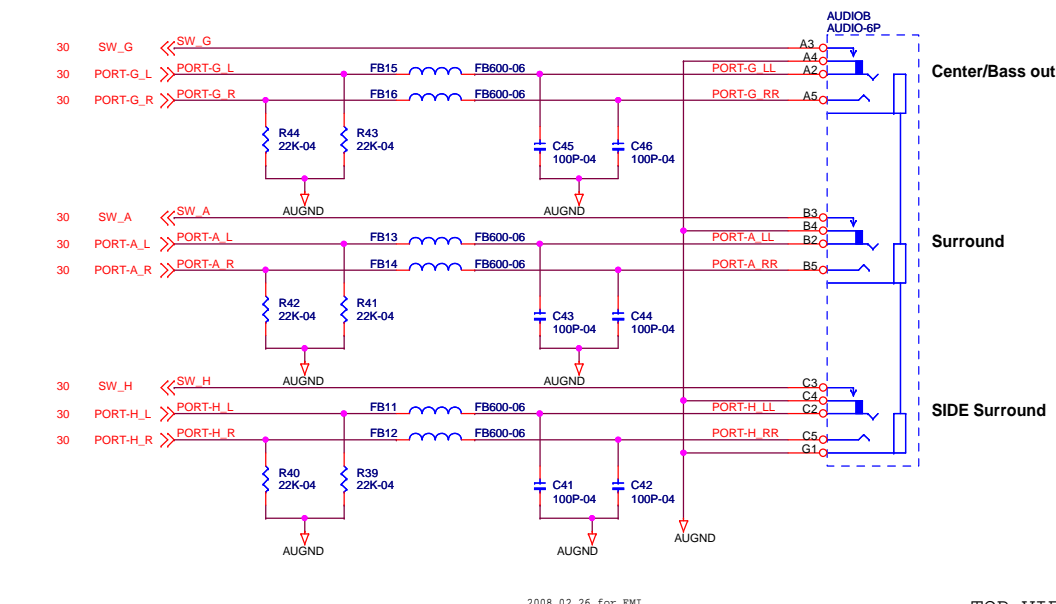
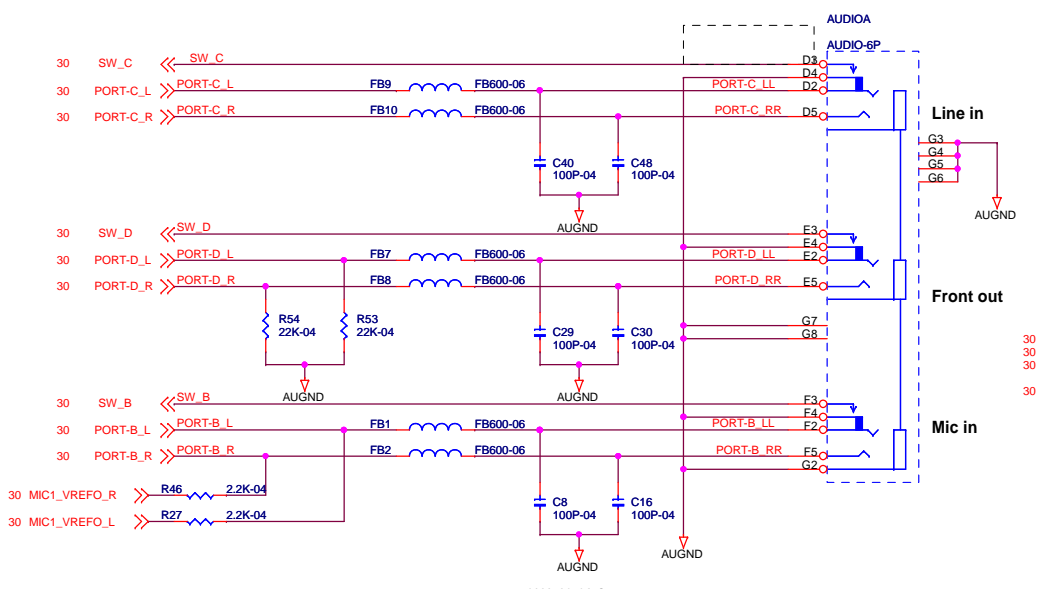


Elitegroup Computer Systems

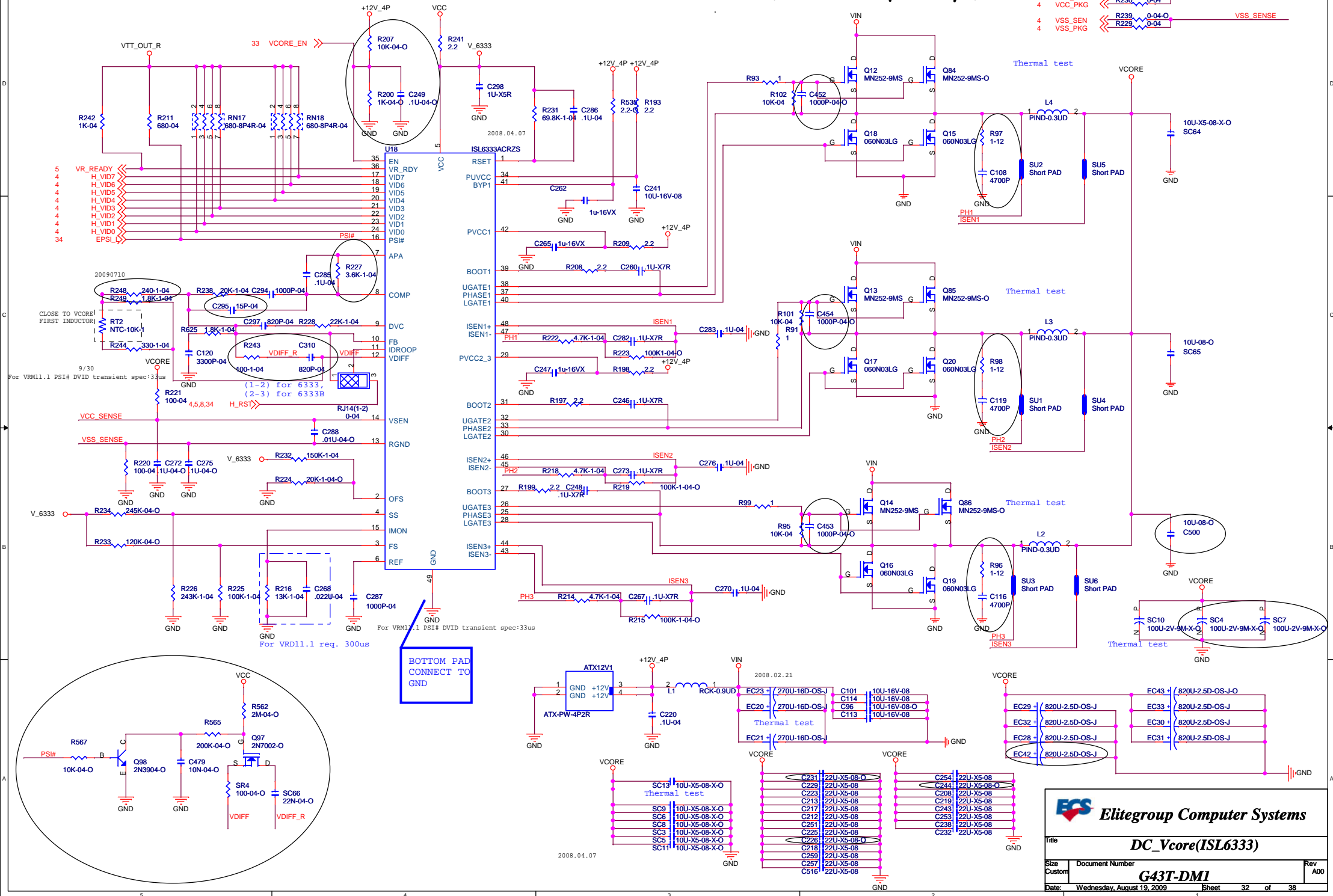
Title: **Audio CODEC(ALC888S)**

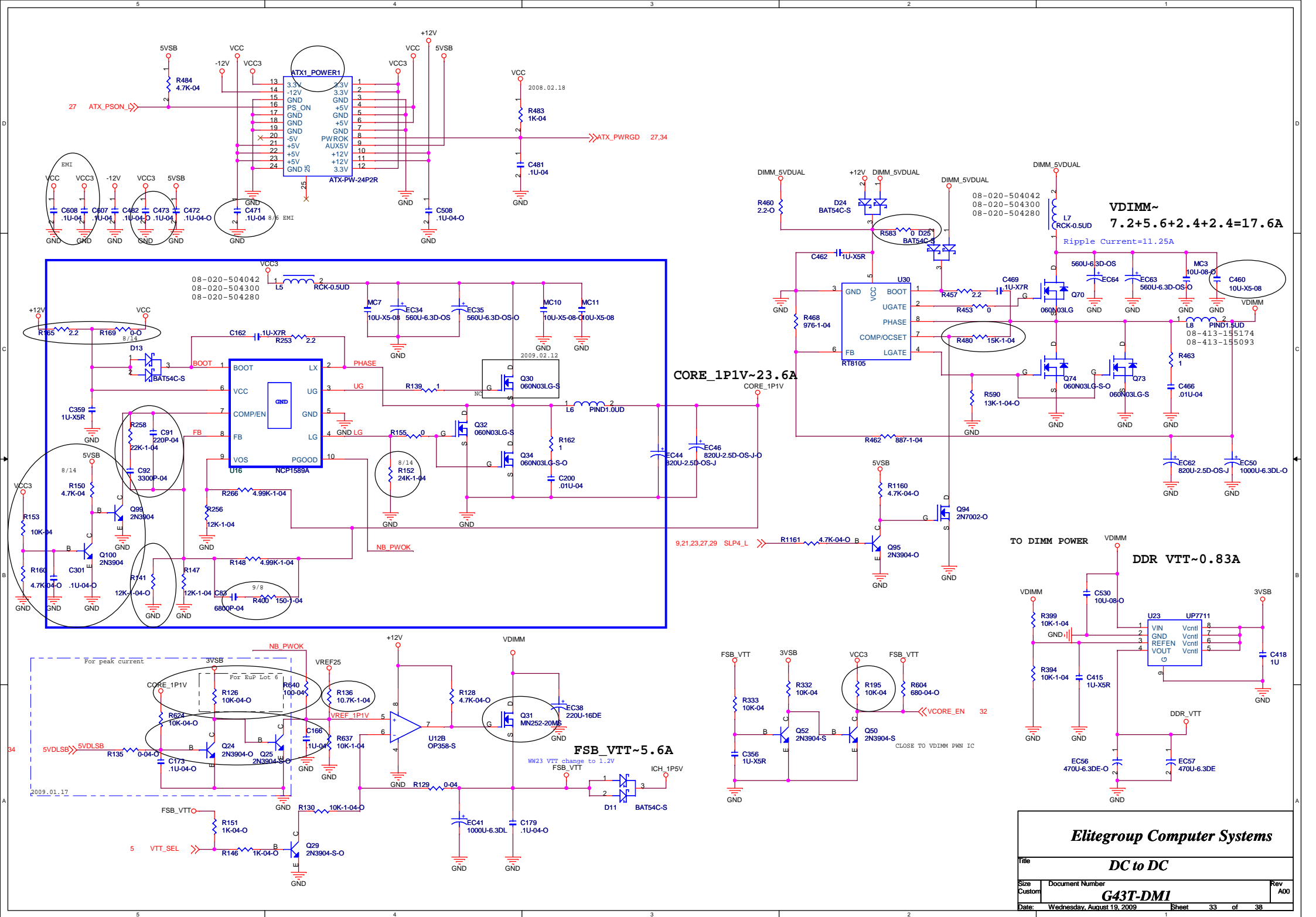
Size: Document Number **G43T-DM1** Rev A00

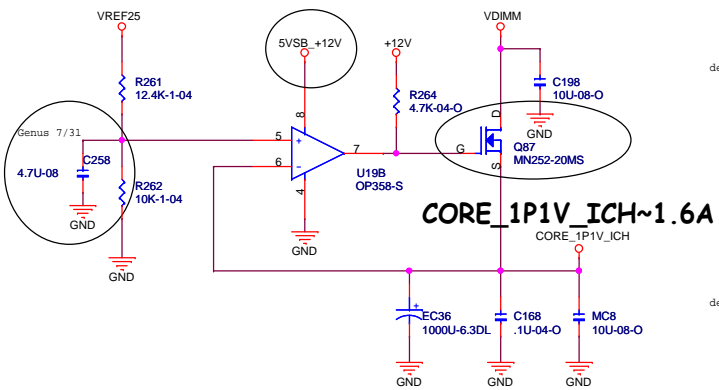
Date: Tuesday, August 11, 2009 Sheet 30 of 38



ISL6333CR FOR VRD11.1 POWER CKT (Low frequency)







If stuff Ra

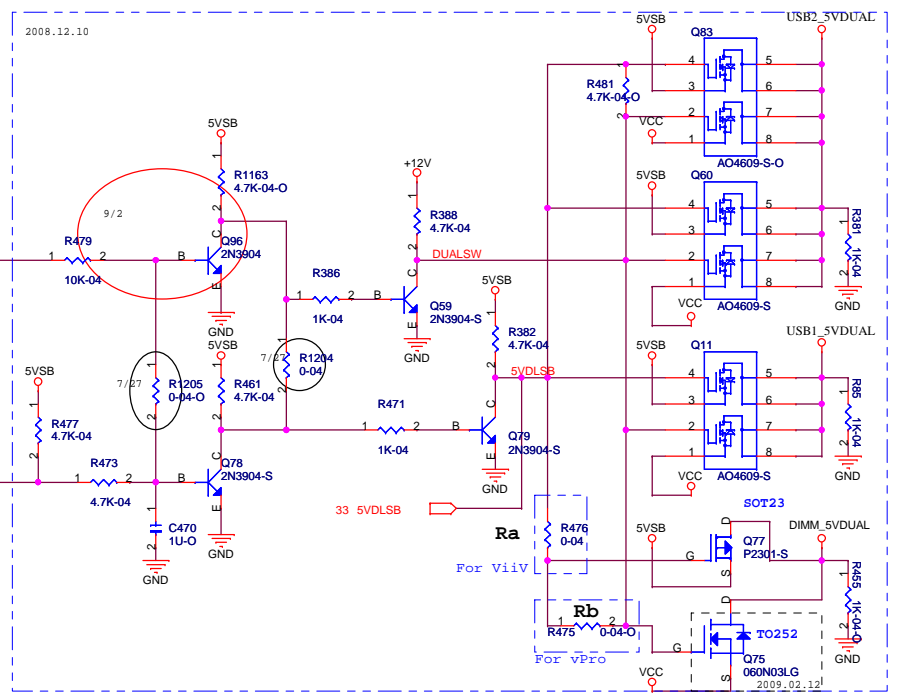
Status	Target			Super I/O 8720-CX
	USB2_5VDUAL	USB1_5VDUAL	DIMM_5VDUAL	
AC plug	0	0	0	GPIO_S4_S5=OD=1
S0,S1	VCC	VCC	VCC	GPIO_S4_S5=1
S3	5VSB	5VSB	5VSB	GPIO_S4_S5=0
S4,S5	5VSB	5VSB	5VSB	GPIO_S4_S5=0
S4,S5	0	0	0	GPIO_S4_S5=1

default *

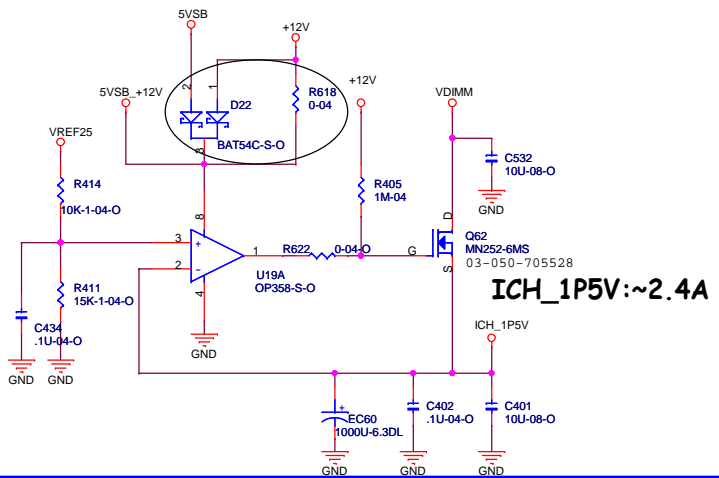
If stuff Rb

Status	Target			Super I/O 8720-CX
	USB2_5VDUAL	USB1_5VDUAL	DIMM_5VDUAL	
AC plug	0	0	5VSB	GPIO_S4_S5=OD=1
S0,S1	VCC	VCC	VCC	GPIO_S4_S5=1
S3	5VSB	5VSB	5VSB	GPIO_S4_S5=0
S4,S5	5VSB	5VSB	5VSB	GPIO_S4_S5=0
S4,S5	0	0	5VSB	GPIO_S4_S5=1

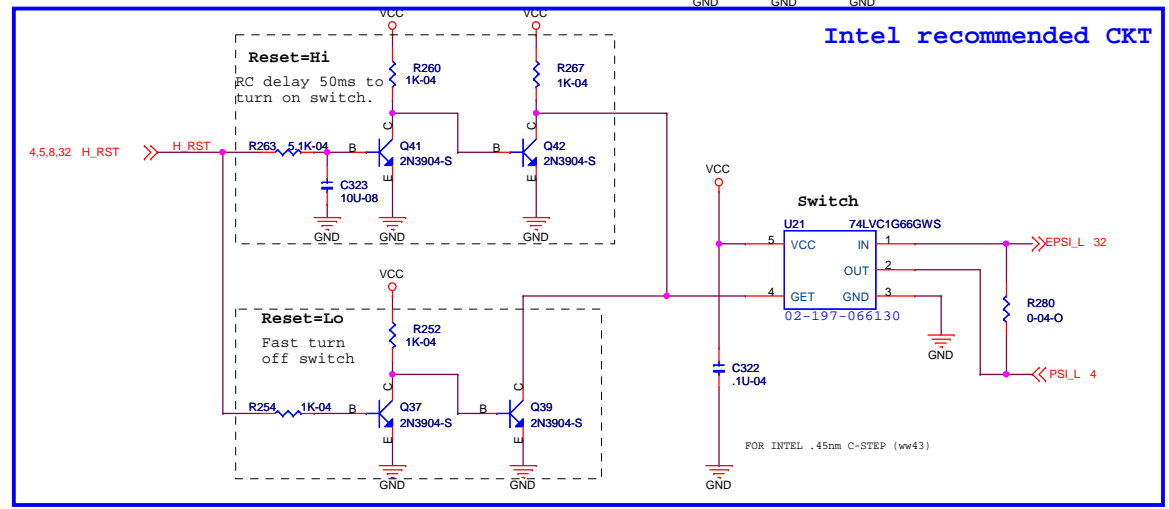
default *



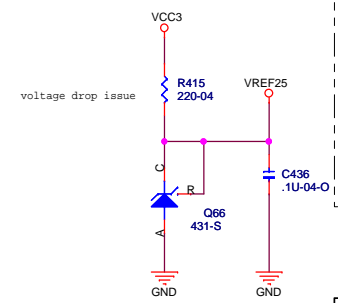
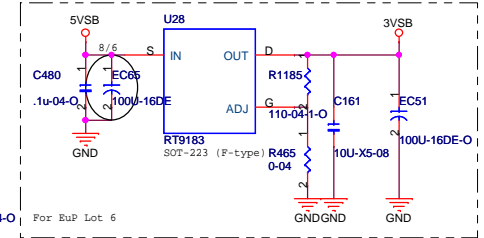
When power off, the ICH_1P5V will be removed



Intel recommended CKT

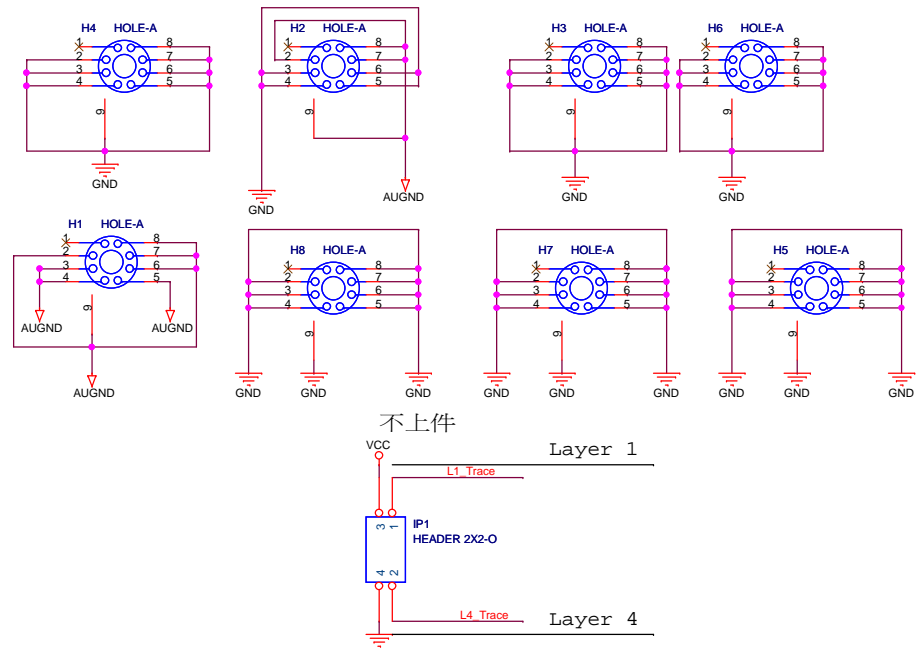
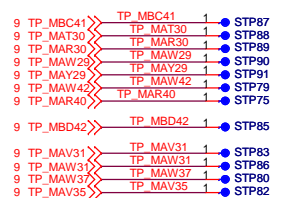
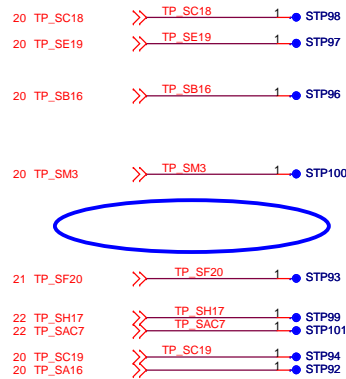
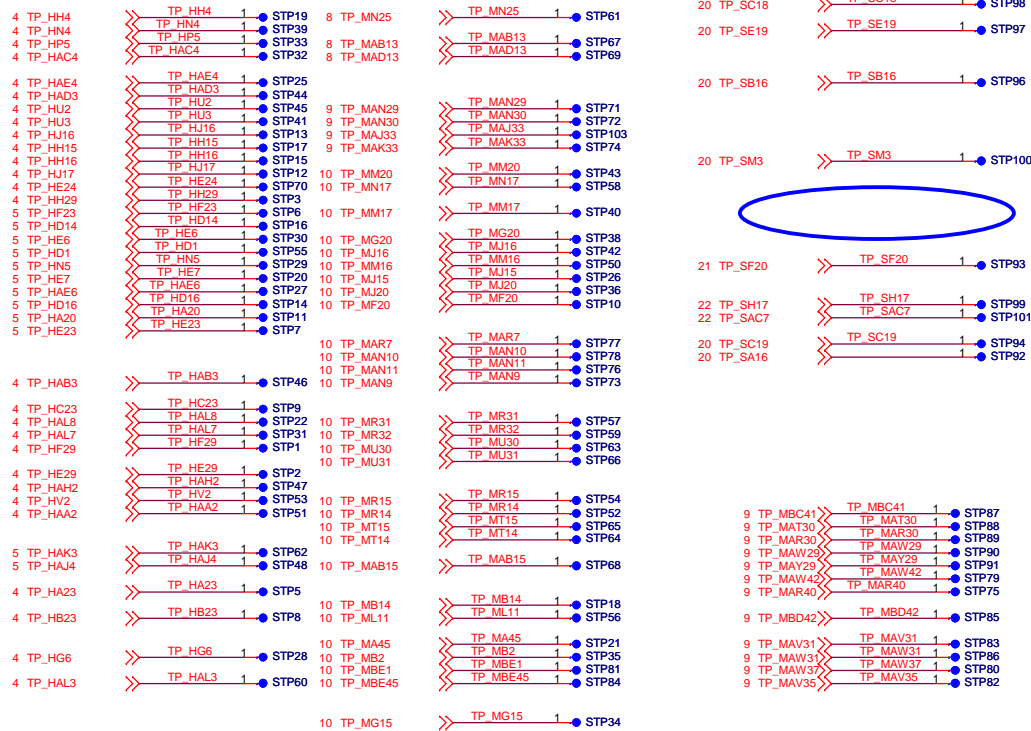


3VSB:1.68A



To VRM IC

From CPU



1080 : trace width 4 mil 50 ohm
 Trace Length 3150 mils
 Spacing: 1.clearance to itself 50/4/50(S:W:S)
 2.clearance to other signal 3W

